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On Single Chip Package for Dual-In Integrated Circuit Packages Called Marriage IC With Switch Tests Simulation.

Frank Appiah

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On Single Chip Package for Dual-In Integrated Circuit Packages Called Marriage IC With Switch Tests Simulation.

Frank Appiah[1], Professional

Abstract. This is about creating a single ic or chip or microchip package on two embedded circuits with their own chip package. This called MarriageIC is shown in article [3] but the main focus here is to switch test the interconnection to functional check the Logic.

Keywords. Single ic, package, Dual-In, switching test, digital ic.

1 Introduction

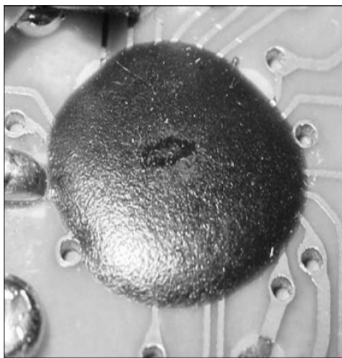
Making note of the various integrated circuit component package types and how they are protected (with metal shielding or encapsulation, for example) is helpful. Some packages allow easy access to the pins in order to probe the device, such as with Dual Inline Package (DIP), Small Outline Integrated Circuit (SOIC), or Plastic Leadless Chip Carrier (PLCC). As the spacing of the pins becomes more dense-as with Thin Shrink Small Outline Package (TSSOP), probing individual pins becomes more difficult without using high-quality probes or a test clip/adapter such as one provided from Emulation Technology (www.emulation.com).

[1] Dr. Frank Appiah is with King's College London, King's Engineers Group Oversea. Contact at appiahnsiahfrank@gmail.com. 2021.

Ball Grid Array (BGA) packaging has all of the device leads located underneath the chip, making it extremely difficult to access the inner pins. It would be necessary to remove the chip and create an extension or adapter board if probing is required. BGA devices are becoming more popular due to their small footprint and low failure rates. The testing process (done during product manufacturing) is more expensive than other package types due to the fact that X-rays are often used to verify that the solder has properly bonded to each of the ball leads.

With *Chip-on-Board* (COB) packaging, the silicon die of the integrated circuit is mounted directly to the PCB and protected by epoxy encapsulation (Figure 1). The "Advanced Techniques" section provides more information on gaining access to and analyzing COB devices.

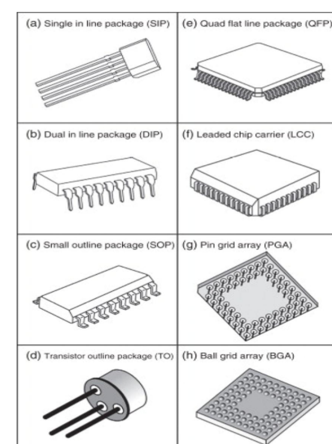
Figure 1: Chip-on-Board. Courtesy Introduction to Digital Logic Design. Copyright © 2002 Syngress Publishing



The goal is to provide an overview of first-level packages for ICs. Keeping in mind that the overall chapter concentrates on microsystem packaging, the focus is more directed toward low pin count packages. Single-chip packages can be categorized by a number of criteria, such as package material (plastic, ceramic, or metal), interconnect arrangement (peripheral or area array interconnects), assembly technology (through-hole or surface-mount technology (SMT)), or package type. Thereby, an industry-wide body, the Joint Electronic Devices Engineering Council (JEDEC, http://www.jedec.org), establishes standard package designators and geometries. In the following, the basic single-chip package types (Figure 2) are briefly discussed (Tummala 2001, Tummala et al. 1997)

Figure 2.

Courtesy of: Allegro® MicroSystems Inc., Worcester, MA, USA.)



Single in line packages: Single in line packages (SIPs) are less common than the dual in line packages (DIPs) and have pins for through-hole assembly only along one side of the package. SIPs are generally plastic packages with a pin count up to 48 and a pin pitch of 2.54 mm.

Dual in line packages: DIPs come in either plastic or ceramic versions and have two rows of interconnects along two opposite sides of the package. The DIP is a commodity through-hole package with up to 84 pins and a most common lead pitch of 2.54 mm (1.78 and 1.27 mm are less common). Ceramic DIPs are frequently used for testing MEMS/microsystem prototypes.

Small outline packages: The small outline package (SOP) is the most common package type for low pin count ICs. It is a lead frame-based plastic package with leads on two sides of the body and pin counts ranging from 8 to 84. The original lead pitch is 1.27 mm (SOP or SOIC (small outline integrated circuit)), but shrink small outline packages (SSOP) with smaller pitches of 0.8, 0.635, and 0.5 mm are available as well. Fully encapsulated SOP with a total package height of less than 1 mm are often termed thin small outline packages (TSOP).

Quad flat packages: Quad flat packages (QFPs) are available as ceramic (CQFP) or lead frame-based molded plastic (PQFP) packages with up to 356 peripheral leads. The surface-mountable QFP has leads on all four sides of the package and lead pitches ranging from 1 mm down to 0.3 mm. QFPs with overall thickness equal or below 1 mm are termed thin QFP or TQFP.

Chip carriers: Chip carriers (CCs) are, like QFPs, surface-mountable packages with peripheral leads on all four sides of the body. In contrast to the QFP with its gullwing leads, CCs feature either J-leads or no leads at all. Leadless chip carriers (LCCs or LLCCs) have a laminated ceramic substrate, leaded chip carriers (LDCCs) with J-leads are either lead frame-based molded plastic packages (PLCCs) or utilize ceramic substrates. CCs are often mounted in dedicated sockets and have I/O counts of less than 120 and typical interconnect pitches of 1.27 and 1.0 mm.

Pin grid arrays: Pin grid arrays (PGAs) are through-hole packages with an area array of interconnect pins using either laminated ceramic (CPGA) or laminated plastic (PPGA) substrates. Pin counts up to 750 are available with pin pitch of either 2.54 or 1.27 mm. CPGA packages are available in cavity-up or cavity-down configurations, i.e., the cavity for the IC is on the opposite or the same side, respectively, as the pin array. Several generations of Intel microprocessors have been packaged using PGAs. More recent versions use a land grid array (LGA), a package similar to the PGA (and BGA (ball grid array)), but having interconnect pads instead of pins.

Ball grid arrays: BGAs are the surface-mountable versions of the PGA with an area array of interconnects with attached solder balls. Plastic BGAs (PBGAs) based on laminated multilayer plastic substrates and ceramic BGAs (CBGAs) based on multilayer ceramic substrates are available. The chip interconnection is accomplished either by wire bonding or by flip chip bonding. Conventional BGAs have a solder ball pitch ranging from 1.0 to 1.5 mm and I/O counts up to 1100 (2600 for flip chip PBGA). Novel chip scale versions of BGA packages, such as Tessera's μBGA (http://www.tessera.com), feature ball pitches down to 0.5 mm, but typically have smaller I/O counts.

Single-chip package development in recent years is driven on one hand by higher and higher I/O counts, demonstrated by flip chip BGA packages with up to 2600 interconnects (see, e.g., Amkor Technologies, http://www.amkor.com), and on the other hand by smaller and smaller package form factors, witnessed by the growth in the area of chip scale packages (CSP). A characteristic of a CSP is a package footprint that is a maximum of 50% larger than the die area and a package perimeter no more than 20% larger than the chip perimeter. An example is the MicroLeadFrame (MLF) package developed by Amkor, a leadframe-based QFP with solderable lands instead of leads, thus also called quad flat no leads (QFNs). Single-chip packages are continuously developing and most up-to-date information on the newest CSP and other packages is found on the packaging manufacturer's and packaging service provider's web pages. The ultimate CSP will have the size of the actual die it protects. In this framework, considerable efforts in the area of WLP should be mentioned (see, e.g., Garrou and Tummala 2001). In WLP, some or all of the packaging steps, such as interconnect formation or encapsulation, are performed

on a wafer level, before the singulation of the wafer into individual ICs. [1] introduces similar WLP concepts for microsystems and MEMS.

The outline of research is to use computer-aided design tooling in creating a chip carrier layout from two dual inline packages. By so doing to show all the pins interconnection circuit used in the chip layout and provide a chip diagram. Then apply a test pattern and also design a switching circuit to test the pattern on an integrated lighting system.

2 Single Chip Layout and Design

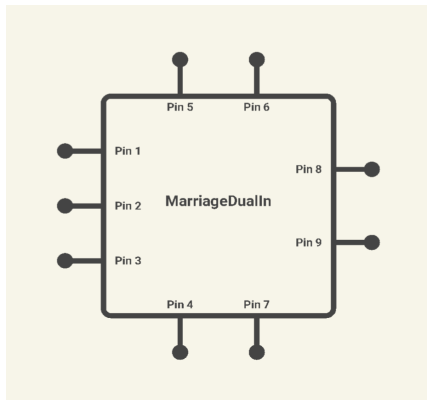


Figure 3. MARRIAGE IC pins

The vivid description of the single ic package is as follows(Figure 3,4,5):
(1) There are 3 inputs to this package,
(2) There are 2 demux inputs to this package,
(3) There are 2 DEMUX select inputs to this package,
(4) There are 2 outputs to this package and
(5) There are 9(3+2+2+2) pins in the package.

The names of the 3 pins are :
Pin 1: DEMUX MbW
Pin 2: DEMUX MbA.
Pin 3: MbNg

Pin	Pin Name
4	DEMUX MbWs
5	DEMUX MbAs
6	MbAMbNg
7	MbANbWs
8	MbAMbngo
9	MbANbWo

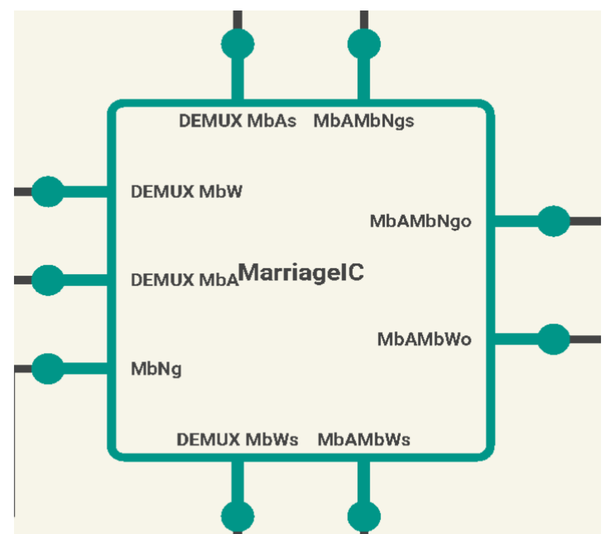
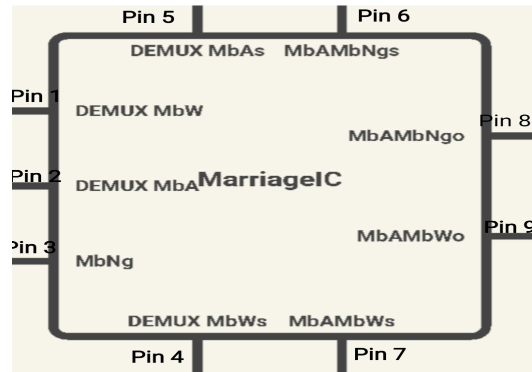


Figure 4. Marriage IC Pin Names

Figure 4. Both Pin and Names IC.



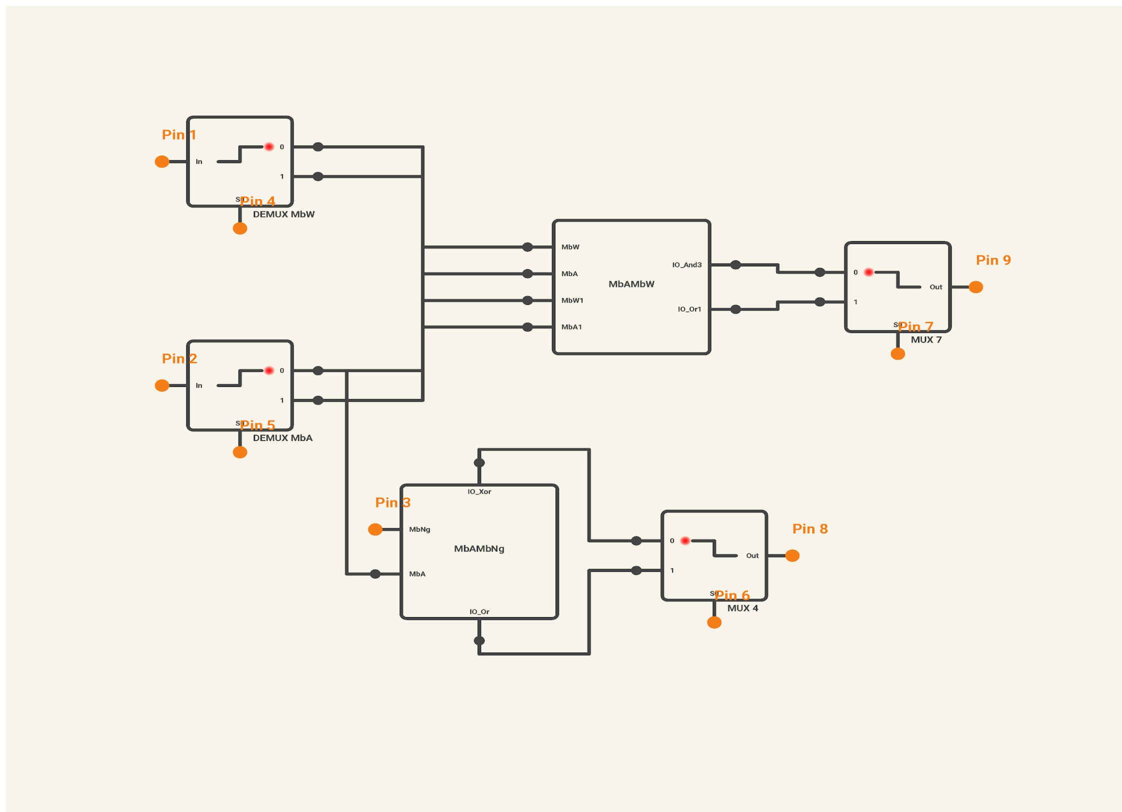


Figure 5: Pins Interconnection Layout

In Figure 5, pins in the interconnection layout were selected by the Logic Circuit Sim Professional tool. In the circuit diagram, the exact pin names are labelled from pin 1 to pin 9. Pin 1 and Pin 4 are connected to demultiplexer (DEMUX MbW) data select input where pin 4 is the select input. For ic MbAMbW, DEMUX MbW is the data input source. Again pin 2 and pin 5 is connected to DEMUX MbA which is sourced as data inputs to MbAMbW ic. For MbAMbNg ic, DEMUX Mba top output is used as an input to MbA pin whilst pin 3 is the other data input.

MbAMbW ic has its output connected or wired to a 2x1 multiplexer, which has pins namely pin 7 and pin 9. Pin 7 of the multiplexer is the data select input. MbAMbW ic

has IO_And3 output selection if pin 7 has a 0 input and IO_or1 output if pin 7 has a 1 input both from the selector. Pin 6 and pin 8 are used on the multiplexer to select the outputs of MbAMbNg ic. Pin 6 is the selector of the data input. With pin 6 having a 0 select input then IO_Xor is outputted in return. Again pin 6 will output IO_or on 1 select input.

3 Switching Test Design

In this section, with the single chip package made as shown above. It is essential not to trust our omen in wishing for a functional logic design but to functional check on several test patterns to correct if needed on error.

Let's look at the test pattern.

Sw: Switch.   State: ON/OFF.

Test name	Sw 2	Sw 3	Sw 4	Sw 8	Sw 9	Sw 10	Sw 11
1	ON	ON	ON	ON	ON	OFF	OFF
2	ON	OFF	ON	ON	ON	ON	ON
3	ON	ON	OFF	OFF	OFF	ON	ON
4	ON	ON	ON	OFF	ON	ON	OFF
5	ON	ON	ON	ON	ON	ON	ON

Switching Test on Test Pattern 1

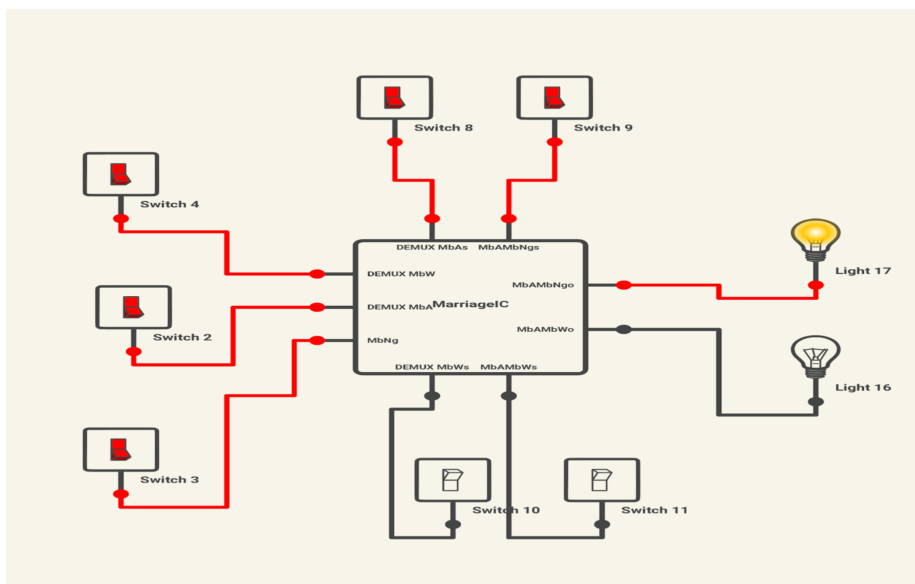
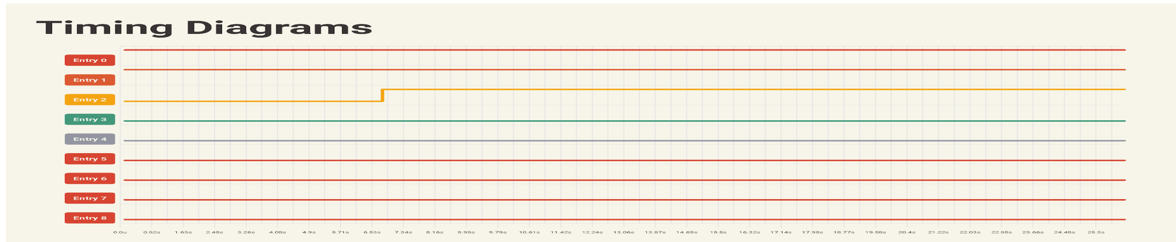


Figure 6: Switch Test circuit

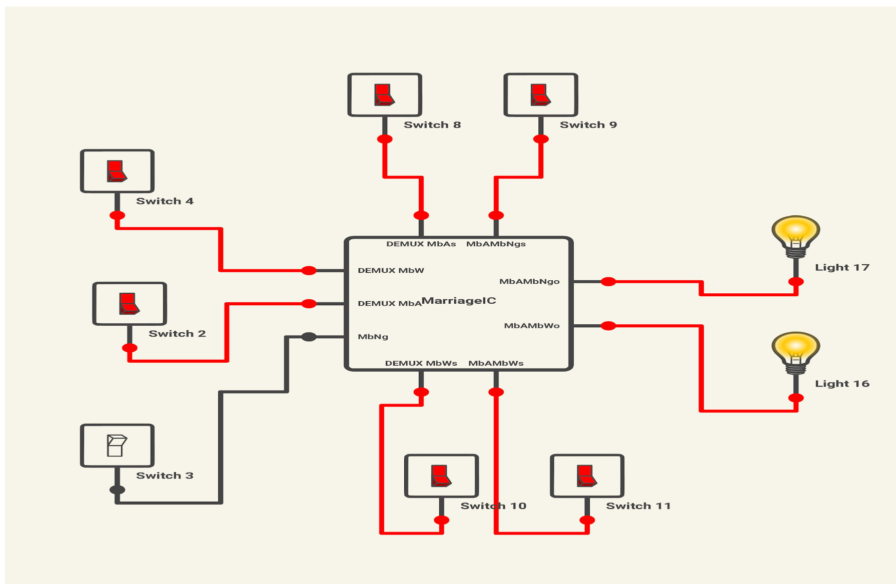
In this test pattern, switch Sw 2 to Sw 9 all have ON States whilst Sw 10 and Sw 11 both have

OFF states. The integrated light circuit brings light 17 on in yellow color. Below is a timing diagram.



Switching Test on Pattern 2

Only sw 3 is off and the rest are all on. With these patterns, both lights comes on that light 16 and 17.



The timing diagram on Simulation is as shown below.

Figure 8

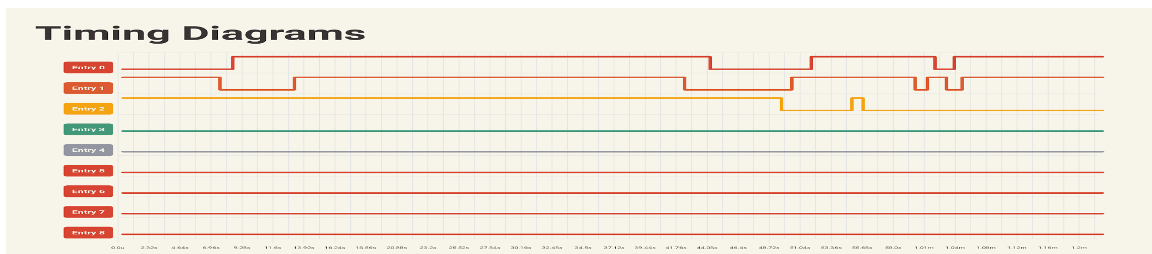
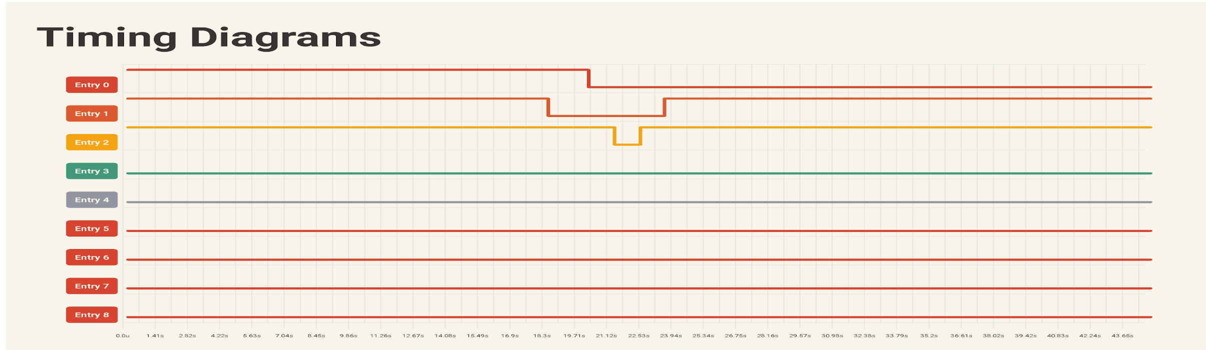


Figure 9: Timing diagram on Pattern 2.

Switching Test on Pattern 3

Figure 10



This circuit implemented test pattern 3 by having switches sw 4, sw 8 and sw 9 in an Off state but have On States for sw 2, sw3, sw 10 and sw 11.

Figure 11: Switch circuit on Pattern 3

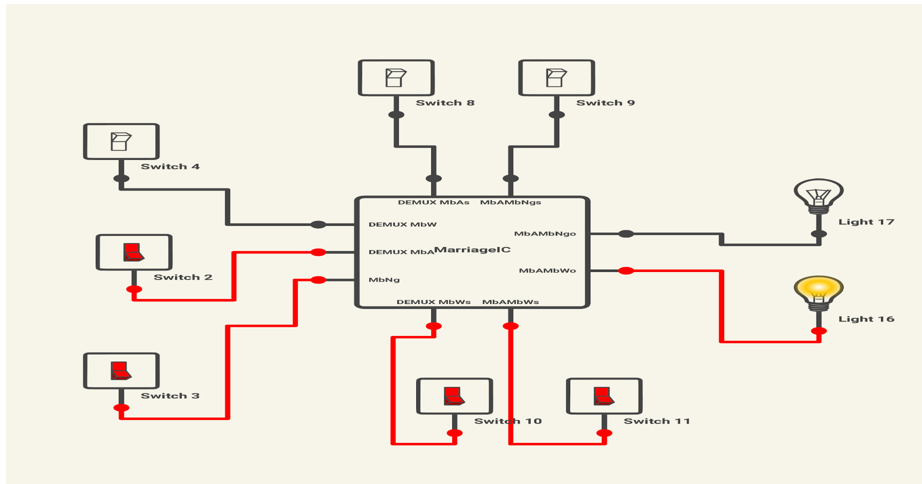
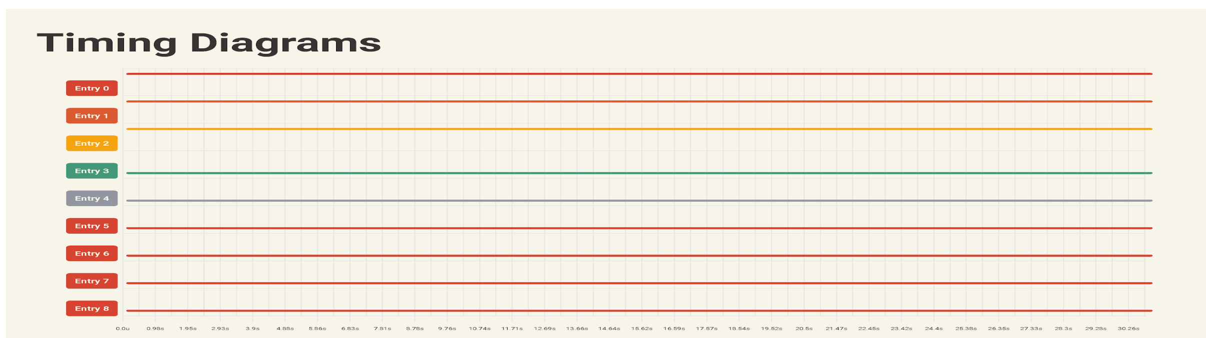


Figure 10 shows the timing diagrams for the switch circuit in figure 11.

Switching Test on Pattern 4



This circuit has both sw8 and sw11 in OFF state. The lights are both Off even having sw2, sw3, sw4, sw 9 and sw 10 in on states.

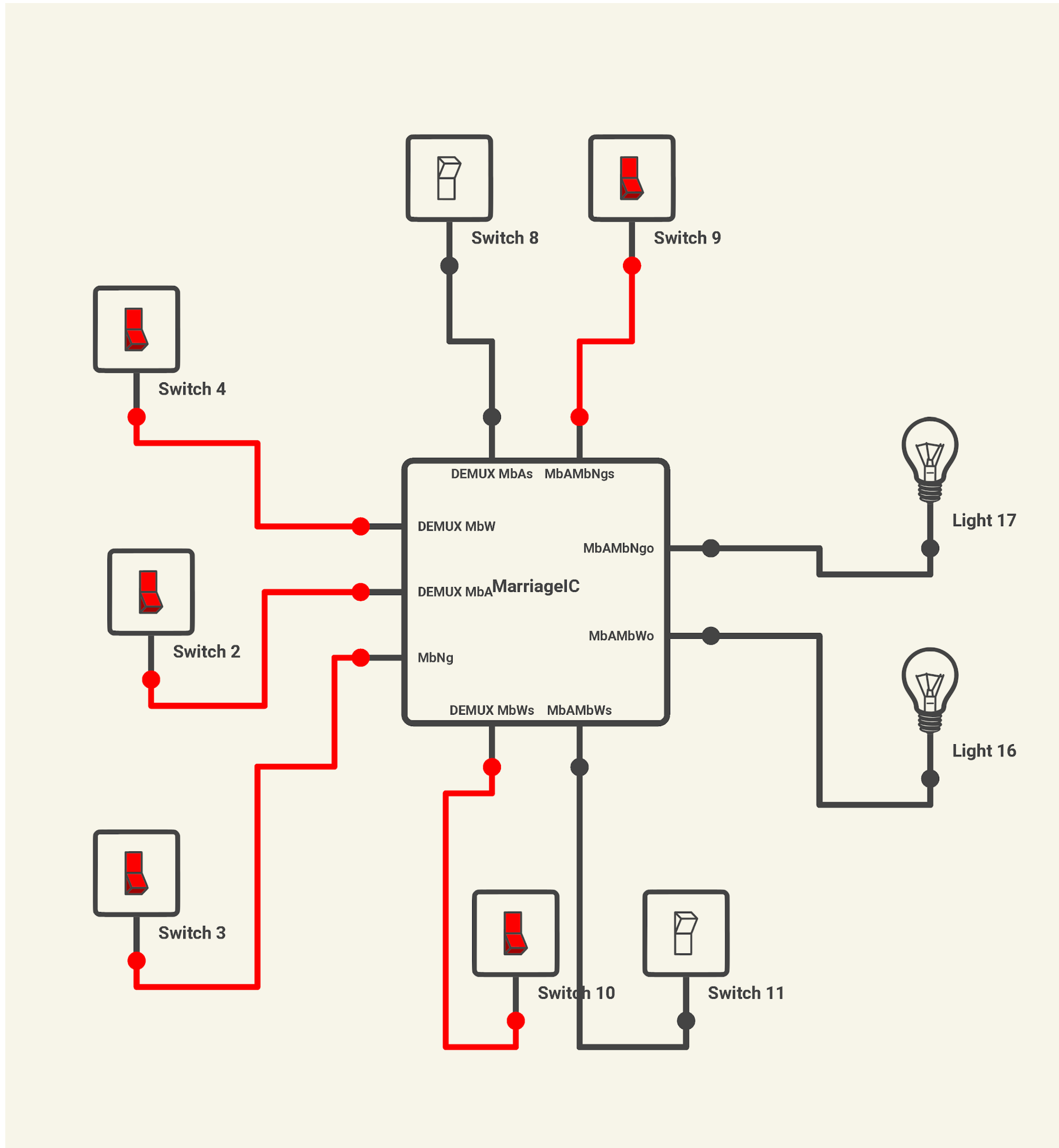


Figure 13.

The timing diagrams are shown in Figure 12 for the circuit in Figure 13.

The final test pattern is based on test name 5.

Test Pattern and Switching Circuit on Test Name 5.

Figure 14.

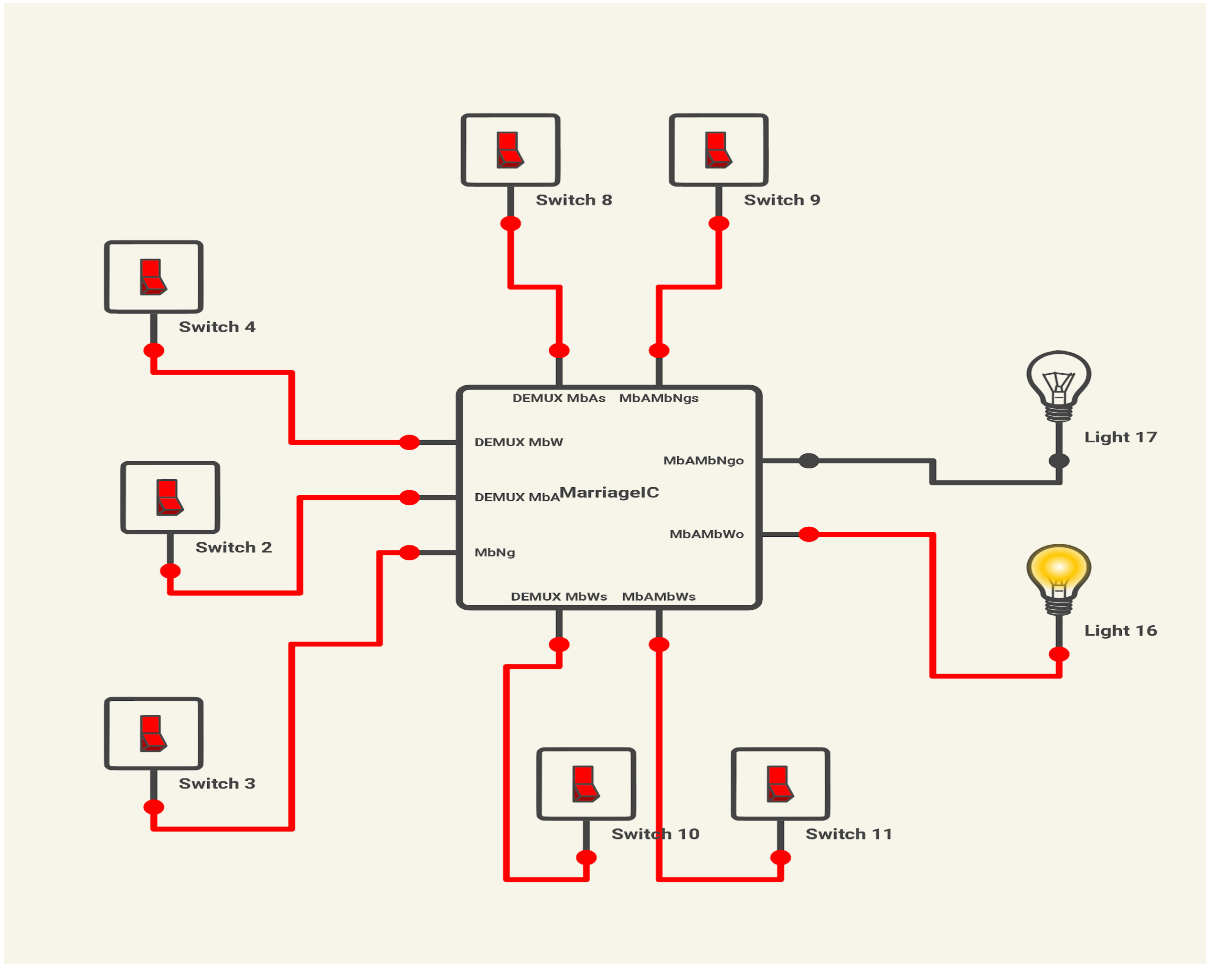
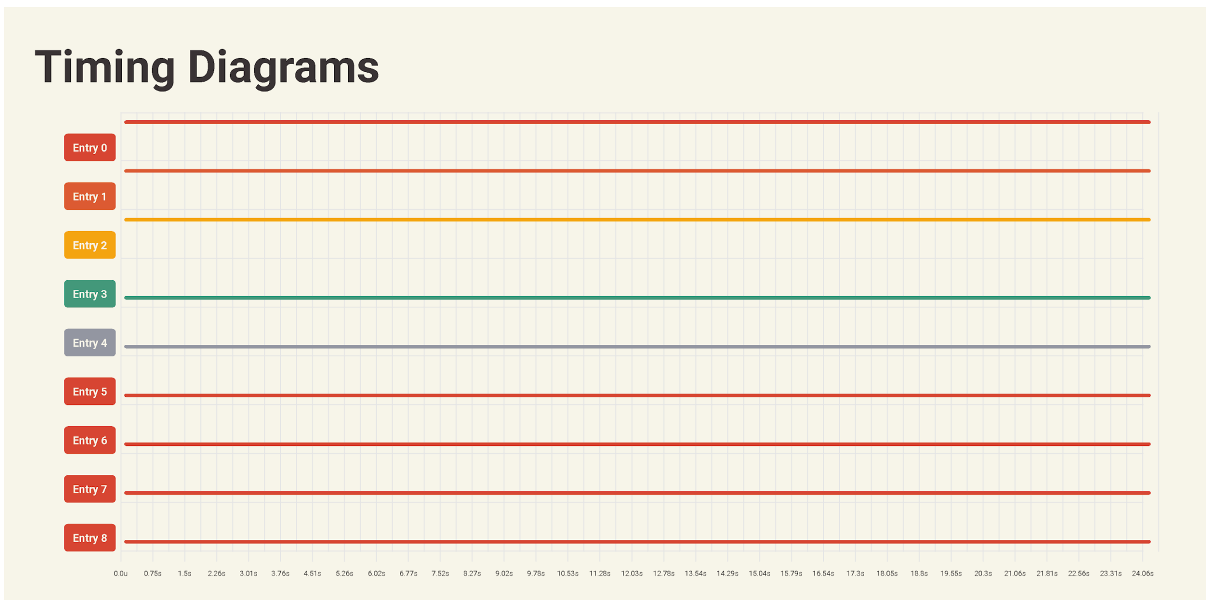


Figure 15.



The test pattern has all the switches in ON State. The output indicates that light 16 comes on and light 17 goes off.

4 Conclusion

This novel work on chip package has originally started as ic Dual-In line package made by computer-aided design tooling into a chip carrier package. The various packages for chip device were looked at but from the 8 device packages only two were exploited - Chip Carrier Package and Dual Inline Package. A step by step approach in computer aided design in integrated circuit is professionally followed. The main focus was to design an experimental ic based on 7 valued logic and embedd its circuit into a chippable piece and further design switching test patterns to show in both verification and validation - A correct functional check by an integrated lighting system.
In total, 5 test patterns for 7 switches were thoroughly tested by switching circuit design based on lighting systems.

Further Reading

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