EasyChair Preprint

№ 15479

Design and Control of Double Interleaved Isolated SEPIC for High Voltage Gain DC/DC Applications

Andrés Nader-Hernández, Antonio Sánchez-Squella,
Rolando Burgos and Patricio Valdivia-Lefort

November 26, 2024

Design and Control of Double Interleaved Isolated SEPIC for High Voltage Gain DC/DC Applications

Andrés Nader-Hernández
Dept. of Electrical Engineering
Universidad Técnica Federico Santa María
Santiago, Chile
andres.nader.14@sansano.usm.cl

Antonio Sánchez-Squella
Dept. of Electrical Engineering
Universidad Técnica Federico Santa María
Santiago, Chile
antonio.sanchez@usm.cl

Rolando Burgos
Center for Power Electronics Systems (CPES)
Virginia Tech
Blacksburg, Virginia, USA
rolando@vt.edu

Patricio Valdivia-Lefort
Electrical Engineering Department
Universidad de Santiago
Santiago, Chile
patricio.valdivia.l@usach.cl

***Abstract*—This paper presents a double interleaved doubler isolated single-ended primary-inductor converter (DVDiSEPIC) designed for high voltage gain in fuel cell systems. Featuring an Input-Parallel Output-Series (IPOS) architecture, the converter achieves significant voltage gain, reduced MOSFET voltage stress, and enhanced efficiency with soft switching. Using a high-frequency transformer and Voltage Doubler (VD) cell, the DVDiSEPIC achieves a voltage gain of 21 under ideal conditions. A cascaded closed-loop control strategy with Proportional-Integral (PI) controllers ensures robust voltage regulation. Comparative analysis highlights the converter's advantages in simplicity and performance.**

***Index Terms*—high voltage gain, soft switching, DCDC converter, isolated DCDC converter, linear control, fuel cell systems**

I. Introduction

Fuel cells (FCs) are a promising alternative to fossil fuels due to the high energy density of hydrogen and low environmental impact, but their adoption is heavily dependent on advanced power electronics due to their inherently low voltage [1], [2]. Key solutions include series-connected fuel cells [3] and customized converters.

High voltage gain converters are one solution to integrate fuel cells into architectures where a DC link feeds loads or other converters. These converters exhibit a significant gain relation between input and output voltage, which can be done with different approaches. For example, in [4] diode-capacitor cells are used to lift the voltage at the output. The authors in [5] propose an isolated solution for renewable energy integration into the grid, in this case a high frequency (HF) transformer is used to realize the isolation between load and source. HF transformers can be key elements in power electronics architectures as the integration to the power electronics stage allows to shrink the transformer. In [6] the concept of soft switching is revised to improve the efficiency of the converter while achieving high voltage gain through inductive coupling.

In this paper, a modified isolated SEPIC (single-ended primary-inductor converter) is used to achieve high voltage gain. The input source is a 65 V PEM fuel cell and the load its fed at 1.4 kV. The circuit exhibits soft switching transitions to enhance the efficiency and a passive regenerative snubber

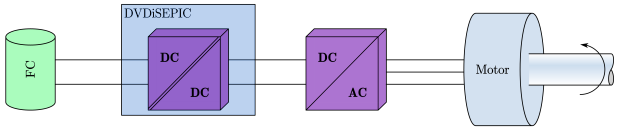


Fig. 1. Power architecture of the system highlighting the proposed converter.

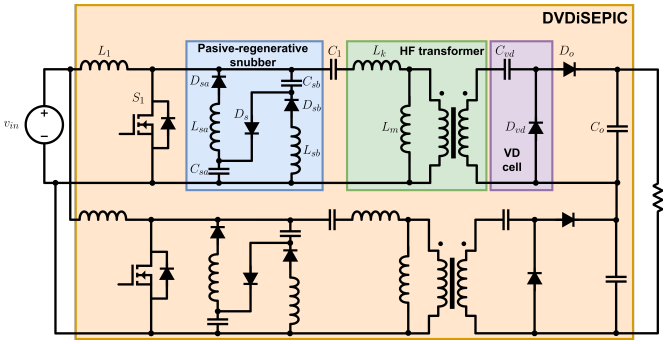


Fig. 2. DVDiSEPIC power topology.

proposed in [7] is used to improve the principal switch voltage stress. This circuit is intended to be used in a two-stage system to feed an inverter that drives a electric motor.

Some works have been done about isolated and non-isolated topologies including several enhancements to achieve better performance with the SEPIC, but they address the situation of voltage reduction in the output, as can be seen in [8], [9]. In this case a high step up converter is analyzed in terms of operation principle and design of the converter parameters.

The rest of the paper is organized as follows: Section II introduces the DVDiSEPIC topology and analysis of ideal operation in steady state. Section III shows a comparison between isolated converters in terms of voltage gain and stress in the main switch. Section IV shows the proposed control strategy based on a cascaded closed loop and simulation results. Finally, in Section V a conclusion of the work is done.

II. Proposed converter topology and design

As fuel cells are the key element in the electrical mobility technology for this investigation, it is reasonable to input their requirements to the converter design [3], [10]: *i*) High efficiency is crucial due to the limited availability of hydrogen, so its preferable to operate with low losses. *ii*) Lesser current ripple in the FC side to enhance the lifespan of the FC in the long run. *iii*) High voltage gain is necessary to match the low voltage of the FC with the DC link voltage. This is a critical point as some manufacturers are testing 800 V drive architectures [11]. *iv*) Small voltage stress in semiconductor devices is needed to improve the reliability of the system and reduce the catastrophic failure rate as low voltages should ensure a safer operation for high switch frequency devices.

In Fig. 1 the power electronic architecture is shown. The system utilizes a two stage approach to deliver power from a FC to a electric motor. This part of the investigation focuses on the isolated DC/DC converter of the architecture, as can be seen in Fig. 2, which employs an IPOS configuration to split input current and double the output voltage. Also, to avoid saturation on the transformer, a VD cell is placed in each channel's output. This cell will create a soft transition in the turn on of the interrupter, improving the efficiency. However, adding this characteristic will increase the complexity of the converter's design and control parameters.

A. Steady state analysis and operation modes

The DVDiSEPIC connects one source to a load increasing the output voltage over the input. To do this, each switching cycle has several sub periods, which can be seen in Fig. 3. In Fig. 4 the ideal operating principle of the converter is shown. The converter has 8 operation modes which are described in the following:

- $(0 - t_1)$ Initially S_1 is turned on and at time $t = 0$ is turned off, this causes the snubber to be charged with current from the transformer, which cannot change its direction instantaneously. This will cause the snubber's capacitors to charge with nearly constant current, so the voltage increases linearly and is reflected in the switch, causing a qZVS turn-off. During this stage the blocking voltage of the output diode starts to decrease. However, it remains blocked.
- $(t_1 - t_2)$ When the transformer finishes discharging all its energy has been stored in the snubber's inductors, the power flow goes from the source to the load through the diode D_o, this can be seen since the output diode current increases and the input inductor current decreases. During this stage the switch voltage reaches its maximum value by means of a sinusoidal waveform, as in the snubber conductors and capacitors conduct, causing a resonance.
- $(t_2 - t_3)$ In this stage the output diode conducts the current coming from the source and the current stored in the snubber's inductors towards the load, during this stage the diode conducts its maximum current according to the following expression:

$$i_{Do} = \frac{1}{n}\left(i_{L1} + 2 \cdot i_{Ls}\right). \tag{1}$$

  During this stage the snubber's diodes conduct and the snubber's capacitors discharge. This stage ends when all the energy stored in the snubber inductors from the transformer is transferred to the load.
- $(t_3 - T_s(1 - D))$ This stage starts with the snubber inductors discharged and the voltage across the snubber's capacitors constant. In this stage there is no conduction in the snubber elements, so the circuit operates as an iSEPIC.
- $(T_s(1 - D) - t_4)$ The fifth stage begins when the switch is turned on. The output diode decreases its current in a linear fashion and the switch increases its current in the

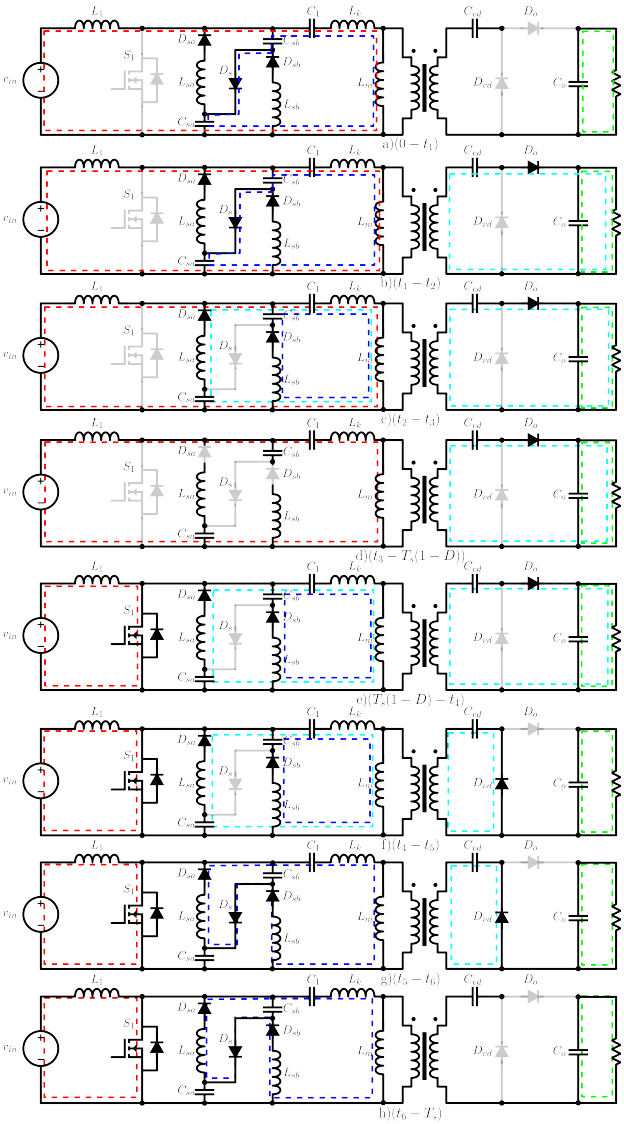


Fig. 3. DVDiSEPIC switching states.

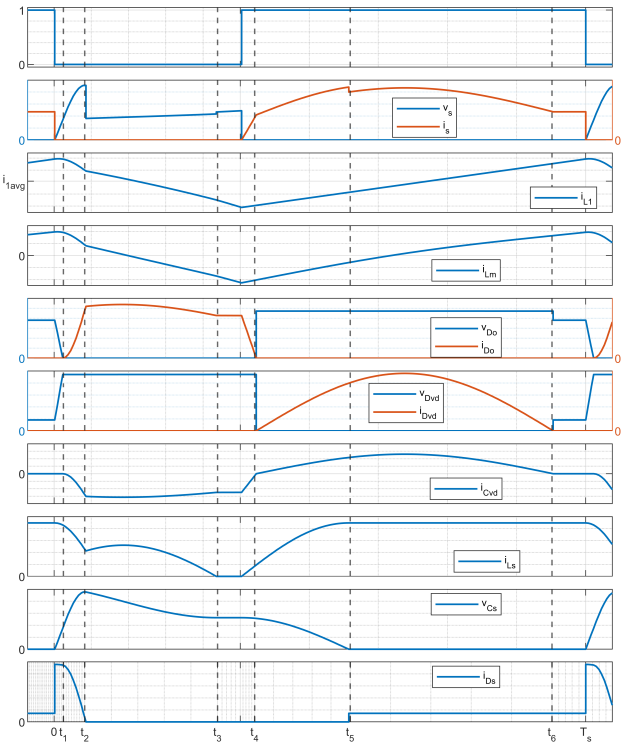


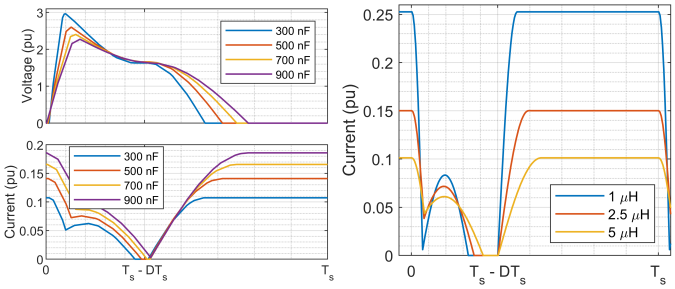
Fig. 4. Electric variables for each switching state for D $>$ 0.5.

same manner, causing a qZCS turn-on. This stage ends when the transformer current becomes zero.

- $(t_4 - t_5)$ This stage begins with the transformer current reversal. This causes a resonant LC circuit to be set up between the leakage inductance L_k, the doubling capacitor C_d and the SEPIC decoupling capacitor C_1, the doubling diode turns on with qZCS. In the snubber, the capacitors are discharged and the inductors are charged, this causes the current of the switch to be affected by this energy transfer and increase until the capacitor C_s is fully discharged. During this stage the output diode is blocked and the power in the load is delivered by the output capacitor.
- $(t_5 - t_6)$ This stage starts with the snubber shorted, so only the VD cell introduces changes in the original iSEPIC circuit. During this subperiod the current in the switch is sinusoidal as well as in the doubler diode and doubler capacitor. As the switch is closed, the input inductor is charged. At the end of this stage the doubler diode is turned off with qZCS, this occurs when the transformer current becomes zero.
- $(t_6 - T_s)$ When the transformer current becomes zero, the current in the switch is constant. At the output, the doubler diode is blocked, so the output voltage is divided between diode D_o and diode D_{vd}. This stage ends when the switch is opened.

B. Passive snubber

For high gain applications the semiconductors can be faced with heavy stress by means of high blocking voltage and



(a) (b)

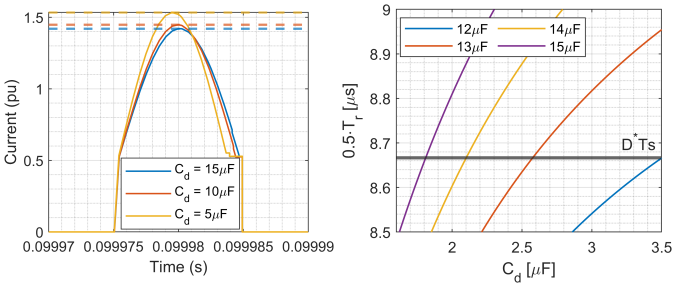
Fig. 5. (a) Effect of capacitor variations on voltage spike and (b) Effect of inductor variations on inductor current dynamics.

conduction current. In this case, the dynamics of the HF transformer have a negative impact on the MOSFET turn off voltage. This effect is related to the leakage current which will change its direction generating a high voltage transition. If this transition is not properly managed, the MOSFET could get damaged or even destroyed during the operation.

To manage the high voltage transitions and protect the MOSFET, a regenerative-passive snubber, as proposed in [7], is included. This snubber reduces the voltage stress by storing excess energy and feeding it to the load, thus enhances the overall efficiency and reliability of the converter. As shown in Fig. 5a), increasing the snubber capacitance lowers the voltage spike, directly reducing the block voltage of the MOSFET since the snubber capacitors are in parallel during the off time. Nevertheless, the increase of capacitance generates a rise in the inductor current. This will increase losses and can cause improper work of the snubber as the inductor would need more time to discharge completely before the next operation stage is reached as can be seen in the purple line of the bottom graph of Fig. 5a).

In Fig. 5b) the changes of the L_s current can be seen based on changes on the inductance. As can be expected, a lower inductance makes all dynamic changes faster. For example, with 1 μH a higher current appears on the inductor, but even in this case the current will reach zero before the next stage. One problem of this is that the high current will increase losses on the snubber. In the other hand, a higher value of inductance will make the current lesser but all dynamics transitions are slower, this can be undesirable if the current is not capable of reach zero value. In that case, the diodes D_{sa} and D_{sb} will never turn off during the operation.

As observed in the parameter effects on the snubber operation, there is a trade off between capacitance and inductance. Capacitance should be maximized to reduce high voltage stress on the MOSFET, while the inductance should also be maximized to minimize current peaks. However, balancing these factors is crucial, as excessive capacitance can increase inductor current and losses, and excessive inductance can slow dynamic responses affecting overall response, potentially preventing the diodes to turn off. To maintain equilibrium prioritization is necessary. In this design the MOSFET is



(a) (b)

Fig. 6. (a) Capacitor effect in switch's resonant current and (b) Capacitor design space for n = 4 and 75 kHz.

a key element, so the capacitance is designed to make the voltage never go high enough to endanger the MOSFET, this is achieved with 300 nF for a 650 V MOSFET. After this, the inductor value can be selected to have the necessary time to turn off the diodes, which is achieved with 5.5 μH.

C. VD cell

As one of the key characteristics of the DVDiSEPIC is to achieve a high voltage gain in the output, gain cells are an attractive option to enhance the static gain. A voltage doubler cell can be placed in the high voltage side of the HF transformer, this will make the cell to handle less current, while achieving a voltage gain of $1/D$ [12]. One important aspect of the operation of the cell is that it will increase the output voltage without adding more turns to the transformer, which will cause an increase in the losses because a longer conductor is needed to implement more turns. Also, the VD cell will complete discharge the transformer, allowing a better use of the core [13].

The operation of the VD cell will create a resonant process which is caused by the interaction of the C_{vd} capacitor, referred as doubler capacitor, with the C_1 capacitor and the L_k inductance of the transformer. The equivalent capacitance during this process can be calculated as

$$C_{eq} = \frac{C_{vd} \cdot \frac{C_1}{n^2}}{\left(C_{vd} + \frac{C_1}{n^2}\right)}. \tag{2}$$

This process will create a sinusoidal waveform in the VD diode, mitigating losses from on-off transitions. In the MOSFET the same waveform will appear during turn on stage, this will also create the conditions for soft turn on, but can increase the peak current as sinusoidal waveform tend to have a larger peak than square waveform. This can be approached from the doubler capacitor design, as its value will impact directly in the peak current. In general, a smaller capacitor will generate a larger peak of current and a larger capacitor will create a lower current peak, as can be seen in Fig. 6a), where a sensibility analysis is made to better understand the capacitor effect on the MOSFET's current. As the doubler capacitor growths in capacitance, it will require more time to complete the sinusoidal trace, this can be seen in Fig. 6a) in the end of the waveform, where the yellow line has the longest constant current value after the sinusoidal form and the blue line has the smallest. This will impose some restrictions over the configuration of the VD cell to make the power circuit works as intended during this process. The resonant time can be computed as

$$\frac{1}{T_r} = f_R = \frac{1}{2\pi\sqrt{n^2 \cdot L_k \cdot C_{eq}}}. \tag{3}$$

The methodology to tune the doubler capacitor is: 1) Select the switching frequency and turns relation of the transformer. 2) Find the duty cycle through the static gain of the converter. 3) Compute $D^* \cdot T_s$. 4) Define candidate values for C_d and C_1. 5) Compute the equivalent capacitance with (2). 6) Find the resonant time with (3). 7) Find C_{vd} and C_1 combinations that achieve $0.5 \cdot T_r < D^* \cdot T_s$.

It can be seen, from the iterative design process, that lower values of C_1 will make the voltage V_{C1} to vary more, producing undesirable effects on the rest of components. Lower values of C_{vd} will increase the current through the MOSFET to achieve the same RMS current in less time. Higher values of C_{vd} will increase the time of the resonant process, producing that the converter operates above resonant frequency as can be seen in Fig. 6a). With the methodology mentioned, four designs are tested to get C_{vd} and C_1 combinations that suit the converter, these operations combinations are made with transformer turn relation 3 or 4, switching frequency 75 or 100 kHZ. In Fig. 6b), the design space is shown for the n = 4 and f_{sw} = 75 kHz case. Every point within the colored lines form a $C_{vd} - C_1$ pair. If the pair is under the black solid line, the design is suitable for resonant operation. Is worth to say that with higher n the duty cycle is lower. Also, for lower switching frequency, the available time for the resonant process is increased and that impacts directly in the value of C_{vd} which can be higher. This is why the 75 kHz design space is more dominant on the 5 to 10 μF for C_{vd} than the 100 kHz. In this point is very important to recall that the duty cycle for one operation point will create a specific on and off time. A smaller on time will make that the resonant process should end quickly in order to secure the complete sinusoidal waveform, this is important because, as the duty cycle impact directly in the voltage gain, some disturbances could make the circuit loose the soft transition capabilities. For example, for n = 4 the duty cycle is lower for the same voltage gain than n = 3, this makes that the capacitor C_{vd} has to be smaller to achieve the completion of the resonant process during the available time, increasing the current.

III. Voltage Gain and Stress

In terms of voltage gain the DVDiSEPIC can be divided into several operational blocks. The first block is the SEPIC circuit itself, which behaves as a non-inverting buck-boost. The second block is the HF transformer, and the third block is the VD cell, the snubber is not consider as its operation

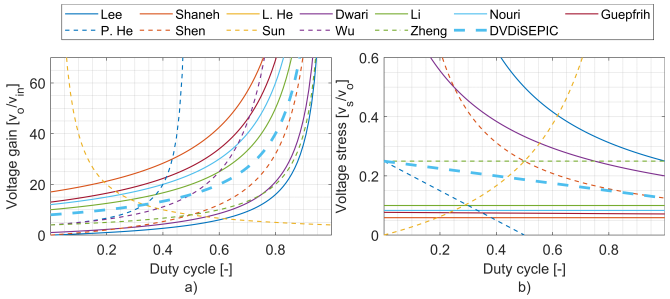


Fig. 7. (a) Voltage gain and (b) Voltage in switch, for different isolated converters.

time is short enough to be despised. Considering these blocks and the IPOS connection, the voltage gain can be obtained as

$$M_{DVDiSEPIC} = 2 \cdot \frac{D}{1-D} \cdot n \cdot \frac{1}{D} = \frac{2n}{1-D}. \quad (4)$$

In Fig. 7a) a comparison of several converters' static gains is presented where, compared with other isolated circuits, the DVDiSEPIC has higher static gain in the lower duty cycle. The DVDiSEPIC has fewer active switches but more passive elements and diodes. This can be advantageous since active switches add more complexity in terms of control and drive circuitry. Nevertheless, it is important to note that the losses may increase as the number of conducting elements in the circuit increases.

The voltage stress in the main switch can be obtained as a function of the duty cycle as shown in (5)

$$VS_{DVDiSEPIC} = \frac{2-D}{2n}. \quad (5)$$

In Fig. 7b) the voltage stress in different isolated converters is plotted. In the DVDiSEPIC topology, the switch experiences increased voltage stress as the duty cycle rises. However, it is crucial to note that the voltage stress calculation does not account for variations in the snubber capacitance, which can reduce the peak voltage experienced by the switch.

IV. Converter Control

The control of the converter is implemented through a cascaded linear control loop per channel. In this case, an independent approach of control is taken, this is, to consider each channel of the converter as a separate and control the variables with independent closed loops.

A. Model acquisition

To extract the dynamics of the DVDiSEPIC an algorithm-based method is used. In this case a combination of data series from PLECS simulation and a zero - pole extraction to form the transfer function of both voltage and current loops was used, as can be seen on Fig. 8a), where the data from the inductor current $i_L(t)$, capacitor voltage $v_c(t)$ and duty cycle D goes from PLECS to the MATLAB toolbox, where the number of poles and zeros is selected to identify the system, with this information the transfer function of the duty cycle to current H_{D2iL} and current to voltage H_{iL2vC} are obtained.

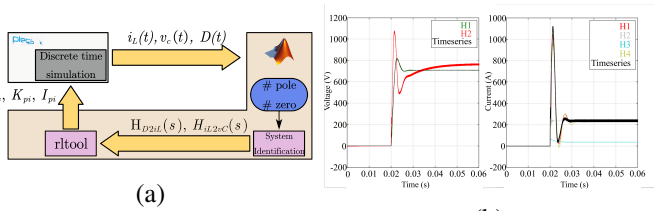


Fig. 8. (a) Controllers obtaining method and (b) Transfer functions step responses.

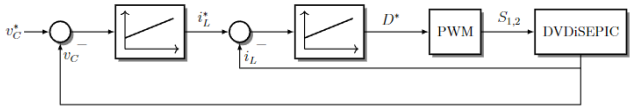


Fig. 9. Control scheme for one channel of DVDiSEPIC.

These functions are then used to tune the controller parameters K_{pi} and I_{pi}.

Model selection is made comparing different outputs of the algorithm with different number of zeros and poles. After, the best candidate is chosen based on a step input compared with simulation data of the circuit at nominal operation. In the left side of Fig. 8b) the duty cycle to inductor current transfer function is observed during a step excitation. The selected transfer function has a 13% error when compared with the simulation and, in the right side of Fig. 8b), current to voltage step response is shown and the selected transfer function has 2% error compared with simulation data.

B. Voltage and current control

The control scheme is shown in Fig. 9. The strategy is to control the voltage at the output capacitors of each channel of the circuit. For simulation purposes the values in Table I are consider.

TABLE I
SIMULATION PARAMETERS FOR DVDiSEPIC.

DVDiSEPIC @ 15 kW and 75 kHz					
L_1	45 μH	C_o	100 μF	C_1	12 μF
V_i	65 V	C_s	300 nF	V_o	1.4 kV
L_s	5.5 μH	D*	0.63	L_m	0.5 mH
n	4	L_k	500 nH	C_d	1.5 μF

Voltage and current control loops are tuned in MATLAB rltool, obtaining the following controller functions which are implemented into the simulation with an anti-windup system

$$C_i(z) = 0.01413 \cdot \left[1 + \left(\frac{1-0.9992}{0.01} \cdot \frac{1}{z-1}\right)\right], \quad (6)$$

$$C_v(z) = 1.1905 \cdot \left[1 + \left(\frac{1-0.99988}{0.01} \cdot \frac{1}{z-1}\right)\right]. \quad (7)$$

In Fig. 10 a transient test can be seen. This test comprise input voltage variations, output voltage set point change, output current disturbances. After the output voltage of one capacitor reaches its nominal value at 0.5 pu in each output

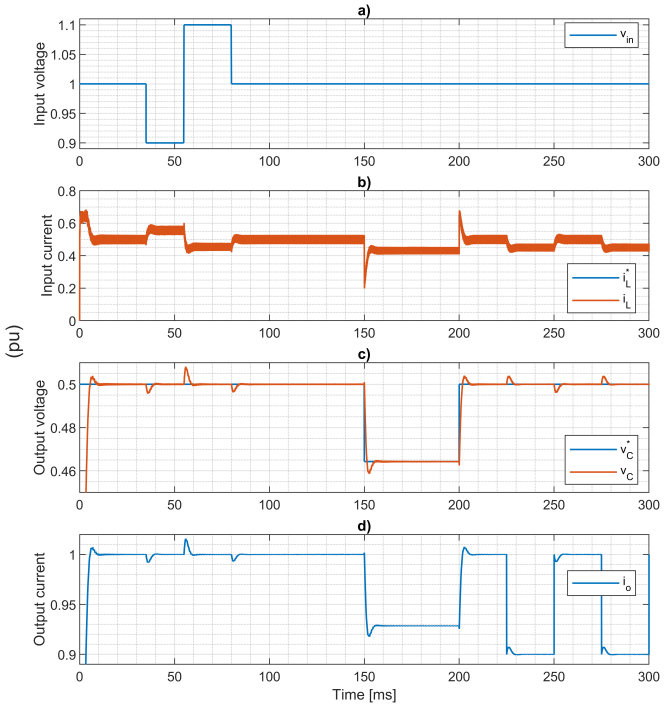


Fig. 10. Perturbations under linear control.

capacitor, the nominal state begins. The first disturbance is an input voltage decrease of 0.1 pu. The input current has to rise to increase the input power and to keep the voltage of the output capacitor constant of its value will decrease. After this, the input voltage raises 0.2 pu, reaching 1.1 pu. Now, the current has to decrease to lower the power or the output capacitor voltage will raise. Finally the input voltage is set to its nominal value.

The next disturbance is a reference change in the output voltage from 0.5 pu to 0.465 pu, this is from 1.4 kV to 1.3 kV. During the transient, a strong change in the input current can be seen from Fig. 10b) at 150 ms. This allows the voltage of the output to drop fast and reach the steady state value in 10 ms with a lower value of 0.46 pu, which is less than 3% undershoot during transient state. The output voltage is set back to its nominal value at 220 ms in a 10 ms transient.

The output current is driven by the output voltage as the load is a resistor. Nevertheless, when an external current is injected in the DC link, the input inductor has to adjust its current to decrease or increase the power from the source to the load in order to mitigate the external current effect. For example, when current is injected into the DC link, the input current decreases allowing the external current to charge the DC link. In the case the current is negative (coming from the DC link) the input current increases to keep the voltage of the output constant.

V. Conclusion

This paper presents a modified SEPIC circuit, specifically designed and tested through simulation for high voltage gain applications within a fuel cell system. The converter forms part of a two-stage system to power an electric motor for traction in electromobility, a scenario that imposes strict conditions and requirements particularly for the fuel cell. The proposed DVDiSEPIC is designed to operate with soft-switching transitions across all its switches at a fixed frequency, allowing to the use of a conventional PWM control scheme. A cascaded control loop design is implemented to ensure output voltage regulation, enabling the system to effectively reject input and output disturbances while maintaining voltage stability under various operating conditions. Ongoing work involves constructing an experimental setup to validate the simulation results and further confirm the practical feasibility of the proposed design while improving the optimization procedure to obtain better performance considering hardware design.

Acknowledgments

This work was supported by ANID Vinculación Internacional FOVI230142.

References

[1] P. K. Seth, B. M. Reddy, and P. Samuel, "Comparative analysis of application of power electronic converters in fuel cell hybrid electric vehicles: A review," in *2018 3rd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT)*, 2018, pp. 1518–1524.

[2] R. Linares, S. Raël, K. Berger, M. Hinaje, and J. Lévêque, "Pem single fuel cell as a dedicated power source for high-inductive superconducting coils," *International Journal of Hydrogen Energy*, vol. 43, pp. 5913–5921, 2017.

[3] R. P. Priya, G. Shivakumar, V. Siddhartha, and A. Edpuganti, "Review of fuel cell power converter topologies for electric vehicles," in *IECON 2023- 49th Annual Conference of the IEEE Industrial Electronics Society*, 2023, pp. 1–6.

[4] K. Li, S.-C. Tan, and R. S. Y. Hui, "Resonant-inductive-boosting dc-dc converter with very high voltage gain." IEEE, 2020, pp. 935–939.

[5] J.-H. Lee, T.-J. Liang, and J.-F. Chen, "Isolated coupled inductor integrated dc-dc converter with non-dissipative snubber for solar energy applications," *IEEE Transactions on Industrial Electronics*, 2013.

[6] M. Abbasi and J. Lam, "A modular sic-based step-up converter with soft-switching-assisted networks and internally coupled high-voltage-gain modules for wind energy system with a medium-voltage dc-grid," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 798–810, 2019.

[7] G. Tibola, E. Lemmen, J. L. Duarte, and I. Barbi, "Passive regenerative and dissipative snubber cells for isolated sepic converters: Analysis, design, and comparison," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9210–9222, 2017.

[8] M. V. M. Ewerling, T. B. Lazzarin, and C. H. I. Font, "A three-level isolated dc-dc sepic converter with parallel-connected output," *International Journal of Circuit Theory and Applications*, vol. 51, no. 3, pp. 1224–1245, 2023. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/cta.3468

[9] M. F. Guepfrih, G. Waltrich, and T. B. Lazzarin, "Unidirectional step-up dc–dc converter based on interleaved phases, coupled inductors, built-in transformer, and voltage multiplier cells," *IEEE Transactions on Industrial Electronics*, vol. 70, no. 3, pp. 2385–2395, 2023.

[10] W. Zhang, L. Xu, J. Li, M. Ouyang, Y. Liu, Q. Han, and Y. Li, "Comparison of daily operation strategies for a fuel cell/battery tram," *International Journal of Hydrogen Energy*, vol. 42, pp. 18 532–18 539, 7 2017.

[11] BOSCH Press DE, "A more efficient drive, a faster recharge," 2023, last accessed 02/07/2024. [Online]. Available: https://www.bosch-presse.de/pressportal/de/en/a-more-efficient-drive-a-faster-recharge-257544.html

[12] B. Andres, L. Romitti, F. H. Dupont, L. Roggia, and L. Schuch, "Analysis and design of isolated sepic converter with greinacher voltage multiplier cell," *Congresso Brasileiro de Automática - CBA*, vol. 2, 12 2020.

[13] B. Andres, L. Romitti, A. M. S. S. Andrade, L. Roggia, and L. Schuch, "Comprehensive analysis of voltage step-up techniques for isolated sepic," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 69, no. 10, pp. 4298–4311, 2022.