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Conducted EMI Mitigation in Transformerless PV Inverters Based on Intrinsic MOSFET Parameters

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Abstract – Electromagnetic interferences (EMI) caused by the high switching frequency of power semiconductors in transformerless single-phase grid-connected photovoltaic (PV) inverters have adverse effects on the lifetime of PV cells and reliability of the electronic and domestic equipment in the neighborhood of the PV installation. This paper proposes a design methodology that helps electronic circuit designers reduce EMI in single-phase PV inverters involving a large number of power semiconductors. Firstly, the most disturbing sources (switching cells) in terms of EMI are identified. Thereafter, a careful choice of the Si-MOSFET assigned to these sources is performed based on its intrinsic parameters. The method is applied to an H5 PV inverter and validated with numerical simulations and experimental tests. The obtained results show a decrease in the conducted EMI after the identification of the disturbing source and the selection of the Si-MOSFET with appropriate intrinsic parameters.

1. Introduction

In recent years, the demand for renewable energies has increased considerably due to population growth worldwide, and the accelerated rate of industrial development. Photovoltaic (PV) energy is considered among the most important green sources thanks to its natural availability and sustainability. Traditionally, PV energy is injected into the grid using a DC/AC power conversion system and a transformer; this latter makes galvanic isolation between the grid and the PV panel to break the ground current loops. However, this component is heavy, bulky, and expensive. To overcome these limitations, new topologies of transformerless PV inverters have been developed to reduce the cost and weight of PV systems and enhance their efficiency as well. Nevertheless, the direct connection of the PV sources to the grid through the power inverter gives rise to an important leakage current flowing in resonant circuits containing parasitic elements. This undesirable current can cause several issues such as Electromagnetic Interference (EMI) problem and safety difficulties [1-2]. Several topologies of single-phase transformerless grid-connected PV inverters are already available in the commercial market or widely developed in the research literature to fix personal safety such as H5 [3], H6 family [4-7], optimized H5 (oH5) [8], and PN-NPC [9]. Compared to the conventional H4 topology, they need more than 4 switches with the aim to decouple the PV panel from the grid through the inverter's ac or dc sides during operation modes where no active power is transferred. However, the use of a higher number of power semiconductors complicates the circuit design and optimization from the point of view EMI mitigation.

On the other hand, recent developments in power semiconductor technologies have contributed to the appearance of faster switching components, which allow power converters to have better performance in terms of power quality and power density. However, characteristics such as the rapid turn-on and turn-off of power switches used in PV inverters (IGBTs, MOSFETs, and fast diodes) give rise to conducted EMI that may affect the lifetime of the PV cells. It may propagate to the neighborhood of the PV inverter through the following paths:

- The DC cabling
- The parasitic capacitors toward the ground of the PV generator and semiconductors components.
- The ground electrode system of electronic devices.

On the other hand, the generated common-mode (CM) currents give rise to radiated electromagnetic noise, emitted by the frame wire of the PV panel and the DC cabling. It may affect and decrease the reliability of the electronic and domestic equipment in the neighborhood of the PV installation [10-12].

Few methods were proposed in the research literature to reduce the conducted EMI in single-phase-grid connected inverters. They are based on the use of extra circuits or the development of variable frequency carriers based on PWM techniques. For instance, a bulky passive EMI filter was used in [13] to block the EMI path. Though EMI filters can provide a significant reduction of conducted emissions, however, they are expensive, bulky and provide additional weight to the conversion system because of the use of common and differential mode inductors. A carrier frequency modulation technique was developed in [14]. However, the use of variable frequency carriers complicates the design of snubber circuits and filters. An auto-screening carrier phase-shift algorithm was proposed in [15] to reduce EMI peaks in single-phase PV inverters connected in parallel. Notice that these methods were limited to the conventional H4 topology with only 4 switches. To the best of our knowledge, the mitigation of conducted EMI has not been addressed in new topologies of transformerless single-phase PV inverters using more than 4 switches. Indeed efforts are still focused on reducing the RMS value of the leakage current, efficiency, reliability, and cost issues [16].

This paper proposes a design methodology to reduce EMI in transformerless single-phase PV inverters that use a large number of power semiconductors. It consists first in identifying the most disturbing EMI source through an analysis of the inverter's operation with the PWM control scheme. Thereafter, an appropriate MOSFET is selected for the corresponding commutation cell. The MOSFET's selection is mainly based on the characteristics of its intrinsic parameters. The proposed methodology is applied and validated with a single-phase H5 PV inverter. Both, numerical simulation based on a high-frequency model and experimental results show that a careful choice of the intrinsic parameters of the MOSFET can effectively mitigate the EMI peaks in the PV inverter.

This paper is organized as follows: Section 2 explains the power topology of single-phase H5 PV inverter and provides a high-frequency model. The proposed method for EMI mitigation is explained and confirmed through numerical simulations and experimental tests in section 3. Finally, section 4 provides some concluding remarks.

2. Power topology and High frequency modelling of the PV inverter under study

2.1 Power topology

The power conversion topology understudy is one of the most popular transformerless single-phase grid-connected PV inverters namely H5 inverter [17]. Compared to the conventional H4 topology, an additional switch is used between the positive (or negative) DC terminal of the inverter and the PV array, as illustrated in Fig.1. This switch allows the reduction of the leakage current appearing in transformerless topologies and flowing through the parasitic capacitors (Cpv) and the ground between the PV terminals and the ac grid/load. This additional switch S5 is turned off during the freewheeling mode of the inverter, which allows decoupling the PV array from the grid and hence reducing the leakage current flowing in between. The five switching cells consist of Silicon MOSFET (Si-MOSFET) transistors, controlled with an unipolar Sine Pulse Width Modulation (SPWM) scheme to achieve a three-level output voltage with reduced switching losses. A Line Impedance Stabilized Network (LISN) is inserted between the inverter's AC terminals and the ac grid/load with the aim to study the conducted EMI. The LISN provides a ground path to the high-frequency noise through resistors R1, R2, and the capacitors in series. Therefore, the common-mode EMI could be deduced from the voltages vR1 and vR2 across resistors R1 and R2. The frequency-domain behavior of the conducted EMI is thereafter deduced by applying the FFT to the time domain results [10].

2.2 High frequency MOSFET's modelling

In order to perform an accurate prediction of the EMI source and reduce its effect, it is essential to discuss the high-frequency behavior of the Si-MOSFET. A typical high frequency (HF) model of the MOSFET is illustrated in Fig.2 showing its four electrodes namely, Source (S), Gate (G), Drain (D), and Bulk or Body (B). The equivalent circuit structure of the Si-MOSFET is a default MOSFET model in SPICE (Simulation Program with Integrated Circuit Emphasis) that takes into consideration all the important static and dynamic characteristics of the MOSFET devices [18-20]. The equivalent model includes:

- Nonlinear current source (I_D) between the drain and source. This current is controlled with the Gate-Source voltage.
- Diodes
- Parasitic resistors (R_G, R_S, R_D, and R_{DS} being the gate, source, drain and drain-source resistances, respectively).
- Gate-source, gate-drain, gate-bulk, source-bulk, and drain-bulk capacitors (C_{GS}, C_{GD}, C_{GB}, C_{BS}, and C_{BD}, respectively).
- Parasitic drain and source inductors (L_D and L_S).

The values of the electrode and inter-electrode parameters (resistances and capacitances) depend on the characteristics and technology of the MOSFET. The intrinsic capacitances are affected by several SPICE parameters such as:

- PB: Bulk Junction Potential, used in the junction capacitance formulation.
- MJ: The Bulk Junction Grading Coefficient of the B-D and B-S junctions and applies to both C_{BD} and C_{BS}.

As for the parasitic inductances, they vary upon the transistor's package.

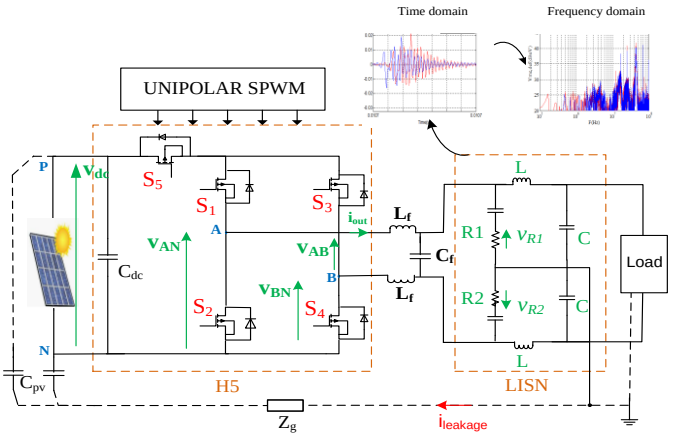

Fig. 1. H5 PV inverter topology connected to the LISN for conducted EMI measurement

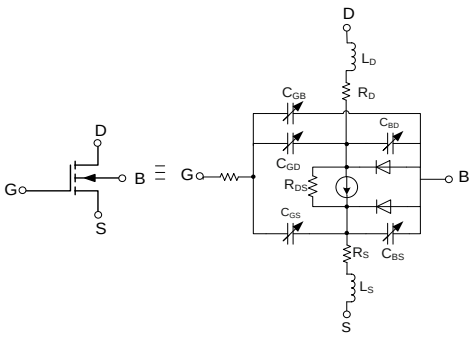

Fig. 2. HF equivalent model of power Si-MOSFET

These intrinsic parameters have an important effect on the EMI provided by the transistor. Indeed, the high-frequency behavior of the MOSFET appears during the commutation process where the fast change in current and voltage across/in the MOSFETs (high dv/dt and di/dt) interact with its parasitic capacitors and parasitic inductors. Thereafter, high-frequency common-mode current spikes are provided. Indeed, high dv/dt across a considerable stray capacitance will increase the amplitude of the high-frequency resonant current flowing through the capacitor. Moreover, high di/dt in a high parasitic inductance will increase the amplitude of high-frequency voltages across the inductor [21-22].
Notice also that a higher value of parasitic resistances contributes to the damping of EMI amplitude. However, this achieved to the detriment of the switching losses. These parameters should, therefore, be carefully chosen to make a compromise between efficiency and EMI provided by the power circuit.

2.3. High frequency PV inverter modelling

A typical high-frequency model of the H5 PV inverter is shown in Fig.3. The conducted electromagnetic emissions provided during the switching operation of power semiconductors, in the form of high-frequency voltages or currents, are coupled to the interfered system through parasitic resistors, capacitors, inductors, and metal wires, of the electronic components and PCB. LS and LD are the parasitic inductances of the drain and the source of the MOSFET that can be obtained from datasheets. Ldc and Rdc are the HF elements of the DC bus capacitors, measured with an impedance analyzer. Cp are parasitic capacitors between MOSFETs and the grounded heatsink. Rp and Lp are the parasitic resistors and inductors of the PCB tracks [23-24]. Their appropriate values depend on the track properties as shown in equations (1)-(2). l, e, and d are the length, thickness, and width respectively of the respective track. ρ is the copper resistivity.

$$R_p = \rho \frac{l}{h \times e} \tag{1}$$

$$L_p = 0.2 \times 10^{-6} \times l \times \left[\ln\left(\frac{2l}{d+e} \right) + 0.5 + 0.22 \times \left(\frac{d+e}{l} \right) \right] \tag{2}$$

The red dotted line shows the path of conducted EMI to the ground through the parasitic elements of the power circuit.

3. EMI mitigation

Static power converters generate polluting interferences over a very wide frequency band. These interferences are provided by both the power stage and the control stage. The state change of digital circuits is the main cause of EMI in the control stage. On the other hand, EMI generated by the power stage are in turn classified into two subcategories:

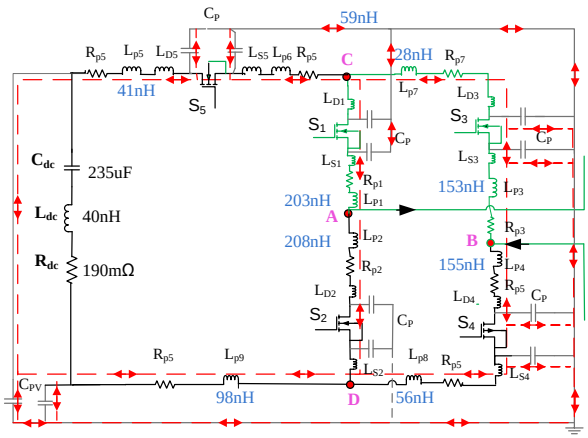

Fig. 3. High-frequency model of H5 PV inverter to estimate the conducted EMI

- EMI due to the commutation with the PWM technique; their amplitude and frequency depend on the power converter topology and the switching technique of power semiconductors.
- EMI due to the transient commutations, their level vary upon the technology and characteristics of power switches.

An overlapping of these parameters' effect exists within a certain frequency band of the harmonic spectra making the analysis of EMI phenomenon caused by the power stage very complex.

In this section, we put forward a method that allows mitigating the EMI caused by the power stage of the PV inverter. It consists of identifying the most disturbing sources from the point of view EMI and selecting the MOSFET transistor with the appropriate intrinsic parameters. Notice that the main motivation behind this objective of EMI mitigation is to reduce their negative impact on the PV cells' lifetime and reliability of electronic equipment in the neighborhood of the PV inverter.

3.1. Identification of the most disturbing source

To identify the most disturbing source in terms of EMI, let us first analyze the modulation process of the H5 inverter. Usually, the unipolar SPWM technique is used to synthesize the target output voltage since it provides less switching losses [3-8]. Therefore, during each commutation period, there exist two operations modes namely active and freewheeling modes. During the active mode, only one switch per leg is turned on. Notice that during the positive half period of v_{AB}, S_1 and S_4 are turned on, while S_2 and S_3 are conducting during the negative half period. Therefore, at the beginning of this active mode, the switch S_5 should necessarily commutate from the off state to the on state to ensure a closed path for the active power transfer from the PV array to the ac load/grid. As for the freewheeling mode of operation, the upper switches S_1 and S_3 are always turned off implying no current is flowing in the DC bus. Therefore, the switch S_5 commutates from the on state to the

off state to decouple the PV array from the ac load /grid. As illustrated in Fig.4, all switches are not commutating during an overall half cycle of the fundamental period of the output voltage v_{AB}. Only the switch S_5 is commutating at any switching period independently of the polarity of v_{AB}. It can, therefore, be concluded that this switch is the most disturbing cell since the number of abrupt variations in the current and voltage in/across S_5 (*di/dt, dv/dt*) is twice as compared to the remaining switches.

On the other hand, a simulation test is performed with the aim to follow the propagation of the resonant current in the H5 power circuit during the commutation process. The proposed HF model of the H5 PV inverter topology (Fig.3) is implemented using a three-level SPICE MOSFET model for each commutation cell. The Si-MOSFET IRFP450 is utilized as the power switch for all commutation cells and the simulation step is set to 5 ns. The remaining simulation parameters are given in Table I. For instance, let us consider a commutation sequence to the active mode state occurring when v_{AB} is positive. Therefore, both S_5 and S_4 are switched on while S_3 is switched off. The results of Fig.5 show there exist one common resonant frequency in the transient currents of all MOSFETs. However, an additional larger resonant frequency appears in the currents through S_5 when it starts the commutation process. Moreover, the most important peak and the larger *di/dt* occur in S_5.

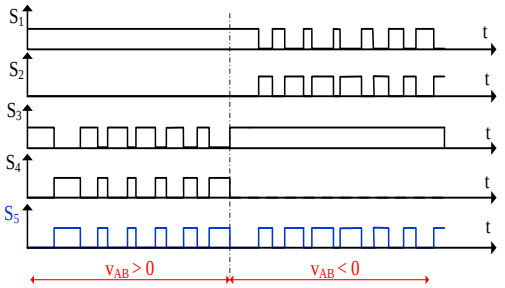

Fig.4. Gates signals of H5 using unipolar SPWM (when S_5 is on state: active mode; when S_5 is off state: freewheeling mode)

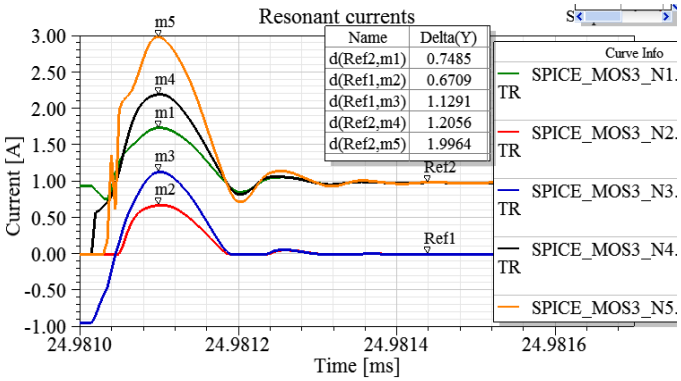

Fig.5. Resonant current in the five MOSFETs of H5 inverter

3.2. Effect of Si-MOSFET intrinsic parameters on the conducted EMI

As discussed in section 2.2, the Si-MOSFET's intrinsic parameters have an important influence on the EMI provided by the switch during commutation. In order to evaluate their effect on H5 inverter topology, simulations tests are carried out where three Si-MOSFETs with different intrinsic parameters are used for S_5. Simulation parameters and operating conditions are listed in Table I. The transistors' references and their intrinsic parameters are shown in Table II. Fig. 6.a illustrates the harmonic spectra of the common-mode emission obtained by applying the FFT to the voltage v_{cm} deduced from v_{R1} and v_{R2} ($v_{cm} = \frac{v_{R1} + v_{R2}}{2}$). The analysis is focused on noise peaks appearing in the frequency band varying from 5 MHz to 30 MHz. As can be seen, a significant change in the common-mode emissions occurs when using transistors with different intrinsic parameters for S_5. The larger amplitude of peaks is obtained with transistor IRFP450. This reference shows large values of the intrinsic parameters L_D, L_S, C_{bd}, Pb, and Mj. Moreover, due to the low values of parasitic resistances, these letter do not provide sufficient damping of the transient oscillations. On the other hand, the lowest amplitude of peaks is obtained with transistor IRF730. Indeed, its resistances R_S, R_D and R_{DS} (ON) are the largest contributing thereafter to better damping of the transient oscillations of the voltage across the transistor.

To emphasize the frequency domain analysis, Fig.6b illustrates the resonant current waveform in S_5 obtained with the MOSFET's references IRFP450 and IRF730. As can be seen, with the reference IRF730, the peak of the resonant current and its transient variation *di/dt* are effectively reduced. Moreover, the first resonance occurring with the reference IRFP450 has entirely disappeared.

Table I - Circuit parameters used in simulation and experimental tests.

Parameters	Value
Input voltage, V_{dc}	40 V
Resistive load	31 Ω
Switching frequency, f_s	20 KHz
Turn on dead time	2µs
modulation index, m	0.8
Bus capacitor C_{dc}	470 µF
Filter's inductors, L_f	5 mH
Filter's capacitor, C_f	6.6 µF
PV parasitic capacitor, C_{PV}	100 nF

Table II–Intrinsic parameters of Si-MOSFETs

	L_S	L_D	R_S	R_D	R_{DS}	C_{gs0}	C_{gd0}	C_{bd}	Pb	Mj
IRFP450	13n	5n	1.45m	0.28	0.33	1.95n	131p	3.38n	3	1.1
IRF740	7.5n	4.5n	8.56m	0.39	0.48	1.39n	147p	1.4n	0.8	0.5
IRF730	7.5n	4.5n	27.9m	0.86	0.75	1.35n	147p	0.7n	0.8	0.5

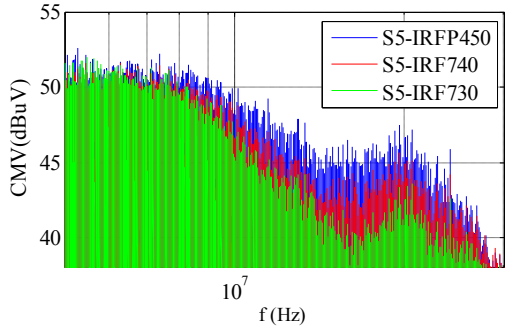

Fig.6.a. Harmonic spectra of the common mode conducted EMI in H5 inverter obtained with numerical simulation

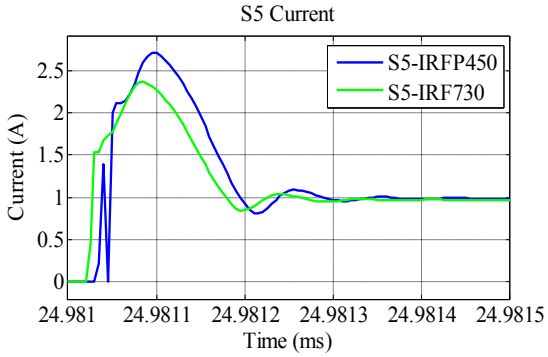

Fig.6.b. Resonant current in S5 obtained with MOSFET's references IRFP450 and IRF730.

3.3. Experimental validation

For validation purposes, an experimental test is carried out using an academic prototype of the transformerless H5 PV inverter. A photo of the experimental platform is shown in Fig.7. The experimental parameters are similar to those used in the simulation. The unipolar SPWM algorithm is implemented using the DSP TMS 320F28335 board and code composer software. The PWM signals are provided by the peripheral output of the DSP and fed to the transistors' gates using the Opto-drivers HCPL3120.

Fig.8 shows the experimental waveforms of the output current and voltage (i_{out} and v_{AB}) confirming the correct operation of the inverter. It illustrates also the voltage across the LISN's resistors (v_{R1} and v_{R2}). The results are obtained with the three MOSFET references of S_5 (IRFP450, IRF740, and IRF730). A zoom in of v_{R1} and v_{R2} show high-frequency transient oscillations that inherently occur during the commutation process and confirming the propagation of conducted EMI to the ac load/grid. The harmonic spectra of the conducted EMI are illustrated in Fig.9. Once more, the lowest amplitude of peaks is obtained with MOSFET's reference IRF730 for S_5 while IRFP450 generates the largest peaks. The perfect concordance between the simulation and experimental outcomes confirms that S_5 has a great effect on EMI provided by the H5 topology. Moreover, the appropriate choice of the intrinsic parameters of only one MOSFET transistor allows effectively mitigating the conducted EMI.

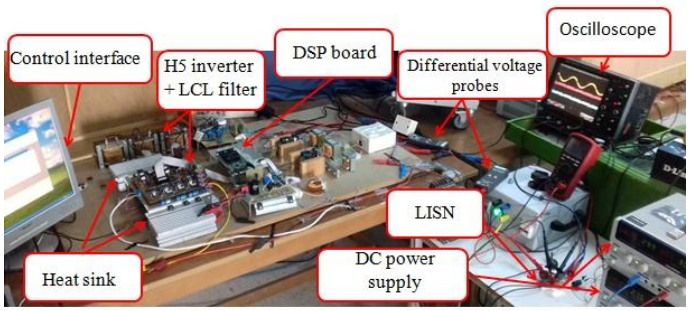

Fig.7. Experimental prototype of transformerless grid-tied single-phase H5 PV inverter

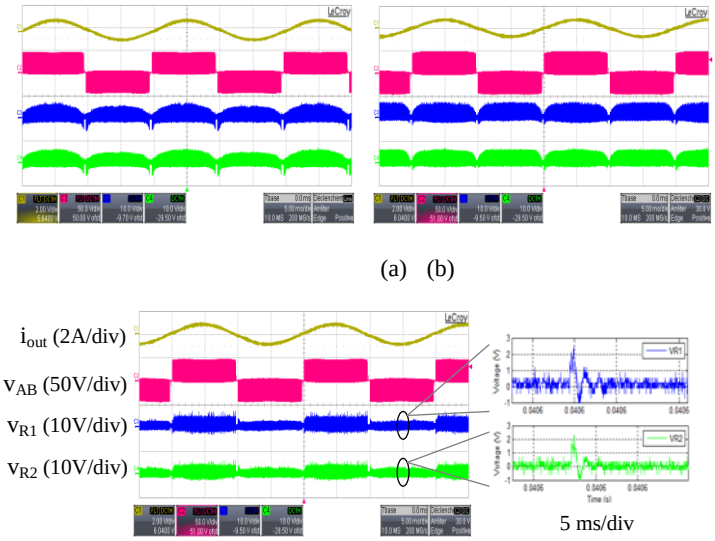

Fig.8.Experimental waveforms of H5 inverter (a) all transistors with IRF740 (b) S5 with IRFP450 (c) S_5 with IRF730

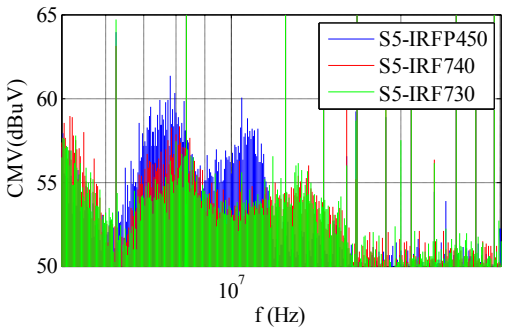

Fig. 9. CM conducted EMI spectra in H5 inverter topology obtained with experimental test

4. Conclusion

This paper proposed a methodology for reducing the conducted EMI provided by a single-phase H5 PV inverter. It consists of firstly in identifying the most disturbing switching cell, which is the additional switch S_5 placed in the DC-bus. Thereafter, the appropriate Si-MOSFET for the switch S_5 is

selected based on its intrinsic parameters. Computer simulations, carried out on a high-frequency numerical model of the H5 PV inverter showed that this method could effectively mitigate the conducted EMI. The results obtained with experimental tests emphasized the same findings. It is therefore recommended to apply this approach at the early stage of PV inverter's design to reduce the negative effect of the PV inverters on the reliability of the electronic equipment in the neighborhood of the PV installation.

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