EasyChair Preprint

№ 940

Fractional Phase Lead Compensation for PIMR-type Repetitive Control on a Grid-tied Inverter

Sainan Chen, Qiangsong Zhao, Xiaolei Wang, Dongyun Wang and Xiaohui Lu

April 28, 2019

Fractional Phase Lead Compensation for PIMR-type Repetitive Control on a Grid-tied Inverter

Sainan Chen[1], Qiangsong Zhao[1], Xiaolei Wang[1] , Dongyun Wang[1,2], Xiaohui Lu[1]
[1] School of Electronic and Information, Zhongyuan University of Technology, Zhengzhou 450007, China
Email: chensainan121121@126.com
[2] School of Intelligent Manufacturing, Huanghuai University, Zhumadian 463000, China
Email: wdy1964@aliyun.com

***Abstract*—Phase lead compensation proportional integral multi-resonant type repetitive control (PLC PIMR-type RC) can improve RC control accuracy and error convergence rate. However, when the sampling frequency is reduced, integer lead phase compensation may result in instability of RC system. To solve these problems, a fractional phase lead compensation PIMR-type RC (FPLC PIMR-type RC) is proposed to improve the steady-state performance and dynamic response. FPLC PIMR-type RC is approximately realized by finite impulse response (FIR) filter. Furthermore, simulation results demonstrate the performance of the proposed control scheme.**

***Keywords*—Grid-tied inverter, current control, finite impulse response (FIR), fractional phase lead compensation, repetitive control.**

I. Introduction

With the sustainable development of new energy, grid-tied inverter, as an interface device for energy exchange between distributed generation units and power grid, has an important impact on the performance of distributed generation systems [1]. Pulse-width modulation (PWM) strategy is commonly used in a grid-tied inverter. Reducing the switching frequency of PWM converter can effectively reduce switching loss, but it will cause the output harmonics to increase [2].

RC can generate high gains at the fundamental frequency and low frequency harmonics, so it has excellent reference signal tracking ability and harmonic signals suppression ability [3]. However, due to the inherent delay of RC, its dynamic performance is poor [4]. Therefore, a proportional integral multi-resonant type repetitive control (PIMR) is proposed [5].

Because RC has phase lag, phase lead compensation can improve system performance. Phase lead compensation provides an angle to compensate the phase lag caused by the plant and low pass filter. The integer phase lead compensation in conventional RC is carried out at high sampling frequency (10 kHz and above), so good results can be obtained [6].

However, integer phase lead compensation PIMR type repetitive control (IPLC PIMR-type RC) at low sampling frequency (4 kHz) will result in overcompensation or undercompensation, which may lead to instability of the system [7]. According to [8], [9], fractional phase lead compensation repetitive control may stabilize the system.

[0]This work is supported by the Foundation for University Key Teacher by Henan Province under Grant 2016GGJS-221, and Interdisciplinary Team of Aircraft Power System and Network Security Technology, Zhongyuan University of Technology.

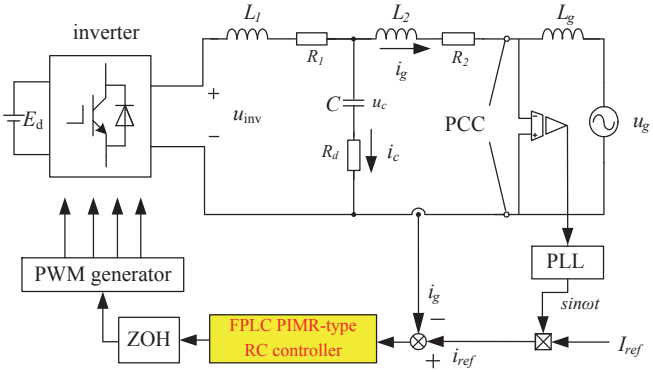


Fig. 1. Block diagram of the FPLC PIMR-type RC scheme.

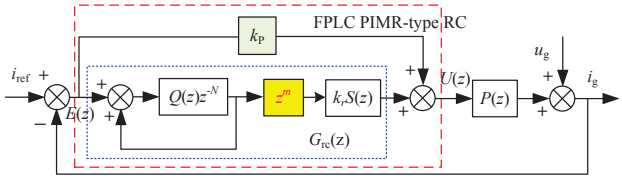


Fig. 2. FPLC PIMR-type RC block diagram.

In this paper, an FPLC PIMR-type RC scheme is proposed for a grid-tied inverter system. The fractional phase lead z^m is introduced, that is, the lead step m is extended from the integer range to the fractional range. To expand the range of parameters, so that the control system design and parameter selection more flexible, the system is more likely to have optimal control performance.

II. Modeling Grid-tied Inverter with the FPLC PIMR-type RC

Fig. 1 shows the block diagram of the FPLC PIMR-type RC scheme, where L_g is the equivalent inductance of the grid; the point of common coupling (PCC) is the common coupling point of grid; u_{inv} is the output voltage; i_g is the grid current and u_g is the grid voltage.

The FPLC PIMR-type RC block diagram is shown in Fig. 2. The proportional gain k_p is used to improve the dynamic response. $Q(z)$ is an internal mode filter or an internal constant. k_r is RC gain. $S(z)$ is a low pass filter. z^m is used to compensate the phase lag caused by the plant and $S(z)$, where

m may be a fraction. Because z^m is a parameter involved in system stability analysis, its design is important.

III. FPLC PIMR-TYPE RC STABILITY ANALYSIS

In Fig. 2, the expression of the FPLC PIMR-type RC is

$$G_{rc}(z) = \frac{Q(z)z^{-N}}{1 - Q(z)z^{-N}} z^m k_r S(z), \tag{1}$$

where m may be a fraction.

The tracking error is

$$E(z) = \frac{1}{1 + [G_{rc}(z) + k_p]P(z)} [I_{ref}(z) - U_g(z)]. \tag{2}$$

Next,

$$1 + [G_{rc}(z) + k_p]P(z) = [1 + k_p P(z)][1 + G_{rc}(z)P_0(z)], \tag{3}$$

where $P_0(z) = P(z)/[1 + k_p P(z)]$.

It can get two stable conditions:
① the roots of polynomial $1 + k_p P(z) = 0$ are inside the unit circle;
② $|1 + G_{rc}(z)P_0(z)| \neq 0$.

By substituting (1) into ②, we can get

$$\begin{aligned} |Q(z)z^{-N}(1 - z^m k_r S(z)P_0(z))| < 1, \\ \forall z = e^{j\omega T}, 0 < \omega < \frac{\pi}{T}, \end{aligned} \tag{4}$$

where $z^N = 1$ [10]. Then, it is assumed that $P_0(z)$ has the frequency characteristic $P_0(j\omega) = N_p(\omega)exp(j\theta_p(\omega))$, where $N_p(\omega)$ and $\theta_p(\omega)$ are amplitude characteristic and phase characteristic, respectively. $S(z)$ has the frequency characteristic $S(j\omega) = N_s(\omega)exp(j\theta_s(\omega))$, where $N_s(\omega)$ and $\theta_s(\omega)$ are amplitude characteristic and phase characteristic, respectively. Using these characteristics, sufficient conditions to hold are

$$\begin{aligned} 0 < k_r < \min_{\omega} \frac{2\cos[\theta_s(\omega) + \theta_p(\omega) + m\omega]}{N_s(\omega)N_p(\omega)}, \\ |\theta_s(\omega) + \theta_p(\omega) + m\omega| < 90^\circ. \end{aligned} \tag{5}$$

IV. IMPLEMENTATION OF FRACTIONAL PHASE LEAD COMPENSATION

According to [11], the fractional phase lead compensation z^d (d is a fraction) is realized by the FIR filter based on Lagrangian interpolation method, as follows,

$$z^d \approx H(z) = \sum_{n=0}^{M} h(n)z^n, \tag{6}$$

where M is the order of filter, when $d \approx M/2$, the interpolation effect is optimal [12]. $h(n)$ is the polynomial coefficient, and n = 0, 1, 2, 3, ..., M.

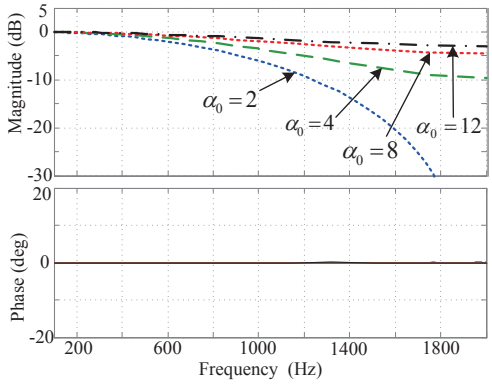


Fig. 3. α_0 takes a different value corresponding to the bode diagram of the filter $Q(z)$.

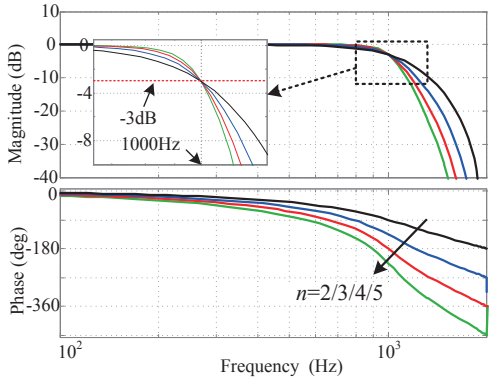


Fig. 4. Frequency response of $2 \sim 5$ order Butterworth low-pass filter.

V. FPLC PIMR-TYPE RC PARAMETER DESIGN

The parameters to be designed of the system are as follows: the proportional gain k_p, the internal filter $Q(z)$, the low pass filter $S(z)$, the RC gain k_r, and the phase lead compensator z^m.

- k_p, $Q(z)$ and $S(z)$

According to the system stability analysis, k_p is chosen to be 15. When the sampling frequency is 4 kHz, the bode diagram of $\alpha_0 = 2/4/8/12$ corresponding to the filter $Q(z) = (z + \alpha_0 + z^{-1})/(2 + \alpha_0)$ is shown in Fig. 3. With the increase of α_0, the filter bandwidth increases. $Q(z) = (z + 8 + z^{-1})/10$ is used.

The frequency response of a $2 \sim 5$ order Butterworth low-pass filter are shown in Fig. 4. As the order of the filter increases, the stop band amplitude decreases faster. $S(z)$ uses a 5 order Butterworth low pass filter. $S_5(z) = (0.0528z^5 + 0.2639z^4 + 0.5279z^3 + 0.5279z^2 + 0.2639z + 0.0528)/(z^5 + 0.6334z^3 + 0.0557z)$.

- k_r and z^m

According to (5), the range of the phase lead compensation m can be determined, and then k_r is determined. By designing an appropriate m, the angle $(\theta_s(\omega) + \theta_{p_0}(\omega) + m\omega)$ is within $\pm 90^\circ$. Fig. 5 shows the bode diagrams of $(\theta_s(\omega) + \theta_{p_0}(\omega) + m\omega)$ with different m. From Fig. 5, the frequency characteristics of $m = 3.4$, $m = 3.5$ and $m = 3.6$ are the same, and

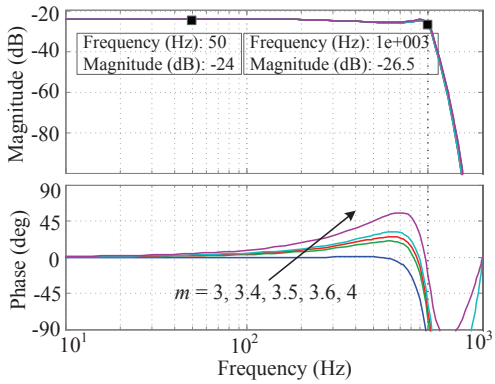


Fig. 5. The bode diagrams of $(\theta_s(\omega) + \theta_{p_0}(\omega) + m\omega)$ with different m.

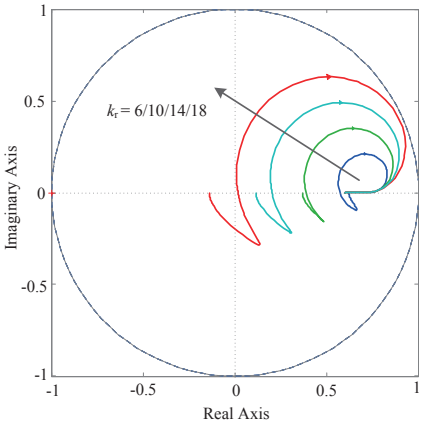


Fig. 6. The trajectory of $H(e^{j\omega T})$ when $m = 3.4$ and k_r takes different values.

the angles of $(\theta_s(\omega) + \theta_{p_0}(\omega) + m\omega)$ are within $\pm 90°$ within 1 kHz. $m = 3.4$ is chosen in this paper.

Definition $H(z) = Q(z)(1 - k_r z^m S(z) P_0(z))$, where $z = e^{j\omega T}$. Fig. 6 shows that the trajectory of $H(e^{j\omega T})$ when $m = 3.4$ and k_r takes different values. $m = 3.4$ enables the RC gain k_r to take a larger value.

VI. FPLC PIMR-TYPE RC SIMULATION

In order to verify the performance of the FPLC PIMR-type RC proposed at low sampling frequency, the simulation was performed in the MATLAB/Simulink. The inverter parameters are shown in TABLE. I.

A. Steady state performance comparison

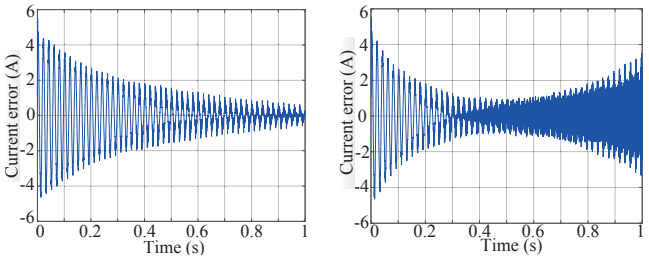
- $m = 3$

When $m = 3$, the current error of the IPLC PIMR-type RC system corresponding to the RC gain k_r of 1 and 6 is shown in Fig. 7. It can be seen from Fig. 7 (a) that the current error convergence time is greater than 1 s, the system dynamic performance is poor. It can be seen from Fig. 7 (b) that the current error starts to diverge at 0.4 s, but the system is unstable.

- $m = 4$ and $m = 3.4$

TABLE I. PARAMETERS DESIGN.

Parameters	Value
Inverter side inductance: L_1	3 mH
L_1 equivalent resistance: R_1	0.48 Ω
Gride side inductance: L_2	2.6 mH
L_2 equivalent resistance: R_2	0.32 Ω
Filter capacitor: C	10 μF
DC bus voltage: E_{dc}	380 V
Grid rated frequency: f_g	50 Hz
Sampling frequency: f_s	4 kHz
Switching frequency: f_{sw}	4 kHz



(a) $kr = 1$ (b) $kr = 6$

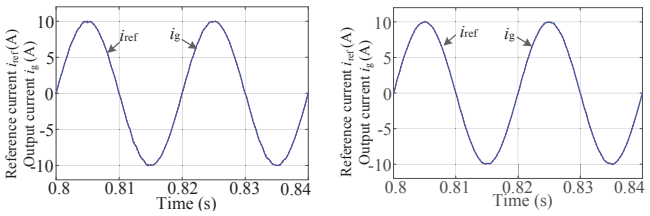
Fig. 7. IPLC PIMR-type RC ($m = 3$) system current error when $k_r = 1$ and $k_r = 6$.

When $k_r = 6$, output current spectrum analysis of IPLC PIMR-type RC ($m = 4$) and FPLC PIMR-type RC ($m = 3.4$) are shown in Fig. 9. Fig. 9 (a) shows that output current THD is 2.12% and the low-frequency harmonic is more than 0.6%. Fig. 9 (b) shows that output current THD is 1.80% and the low-frequency harmonic is less than 0.3%. When $k_r = 6$, control system of IPLC PIMR-type RC ($m = 4$) and FPLC PIMR-type RC ($m = 3.4$) current error convergence is shown in Fig. 10. Fig. 10 (b) shows that can be seen that when the current tracking error tends to be stable, the error is within ± 0.2A, whereas Fig. 10 (a) shows that the error remains within ± 0.4A.

When $k_r = 7$, IPLC PIMR-type RC (Fig. 11 (a)) system output current error gradually converges and then gradually diverges, indicating that the system begins to become unstable. However, FPLC PIMR-type RC (Fig. 11 (b)) system output current error can converge to steady state at 0.1s, and the convergence speed is faster than $k_r = 6$. The current error convergence of trajectory of FPLC PIMR-type RC ($m = 3.4$) control system with $k_r = 10$ is shown in Fig. 12. It shows that output current error can converge to steady state at 0.1s, and the convergence speed is faster than $k_r < 10$. The output current spectrum analysis of trajectory of FPLC PIMR-type RC ($m = 3.4$) control system with $k_r = 10$ is shown in Fig. 14. It shows that output current THD is 2.00%.

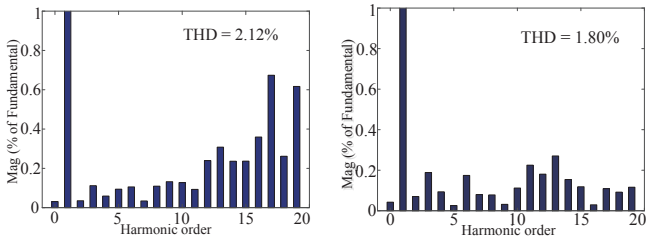
B. Dynamic performance comparison

When the amplitude of the reference current increases from 5A to 10A at 0.5s, the dynamics of the current error of IPLC



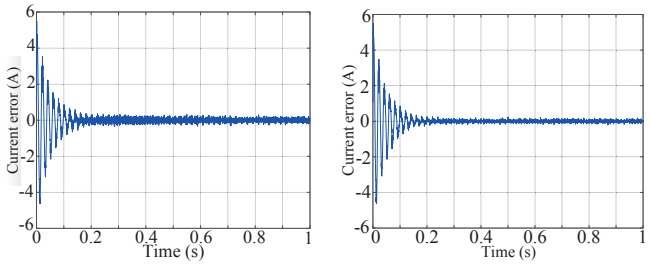
(a) $m = 4$ (b) $m = 3.4$

Fig. 8. Control system reference current and output current (0.8s∼0.84s) when $k_r = 6$: (a) IPLC PIMR-type RC ($m = 4$), (b) FPLC PIMR-type RC ($m = 3.4$).



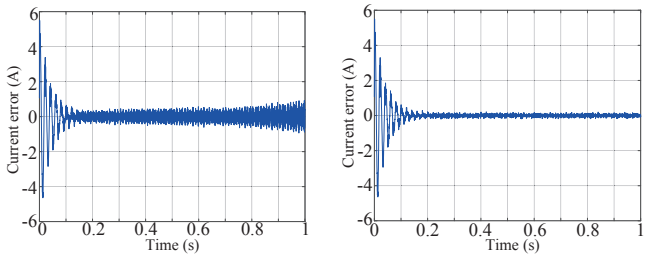
(a) $m = 4$ (b) $m = 3.4$

Fig. 9. Output current spectrum analysis of the control system when $k_r = 6$: (a) IPLC PIMR-type RC ($m = 4$), (b) FPLC PIMR-type RC ($m = 3.4$).



(a) $m = 4$ (b) $m = 3.4$

Fig. 10. Current error convergence of the control system when $k_r = 6$: (a) IPLC PIMR-type RC ($m = 4$), (b) FPLC PIMR-type RC ($m = 3.4$).



(a) $m = 4$ (b) $m = 3.4$

Fig. 11. Current error convergence of the control system when $k_r = 7$: (a) IPLC PIMR-type RC ($m = 4$), (b) FPLC PIMR-type RC ($m = 3.4$).

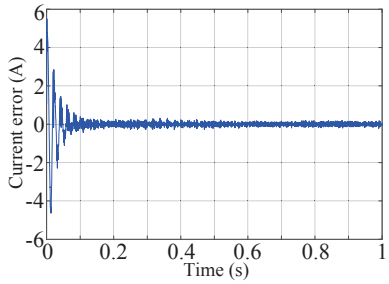


Fig. 12. The current error convergence of trajectory of FPLC PIMR-type RC ($m = 3.4$) control system with $k_r = 10$.

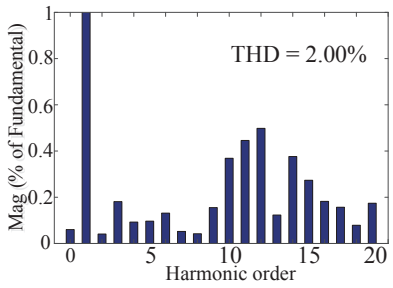
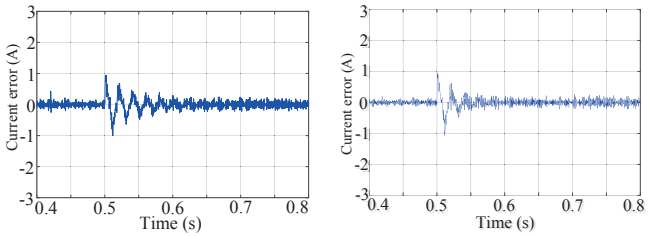


Fig. 13. The output current spectrum analysis of trajectory of FPLC PIMR-type RC ($m = 3.4$) control system with $k_r = 10$.

PIMR-type RC (a) and FPLC PIMR-type RC (b) are shown in Fig. 14. It can be found that the error convergence rate of the FPLC PIMR-type RC is better than IPLC PIMR-type RC.



(a) (b)

Fig. 14. Control system output current error (from 5A to 10A): (a) IPLC PIMR-type RC; (b) FPLC PIMR-type RC.

VII. Conclusion

In this paper, the principle of phase lead compensation is given, the problem of integer phase lead compensation at low sampling frequency is pointed out, and the implementation method of fractional phase lead compensation is given. Finally, it is verified that FPLC PIMR-type RC has better steady state and dynamic characteristics than IPLC PIMR-type RC.

References

[1] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of control and grid synchronization for distributed power generation systems," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1398–1409, Oct 2006.

[2] F. Blaabjerg, Y. Yang, D. Yang, and X. Wang, "Distributed power-generation systems and protection," *Proc. IEEE.*, vol. 105, no. 7, pp. 1311–1331, July 2017.

[3] P. M. de Almeida, J. L. Duarte, P. F. Ribeiro, and P. G. Barbosa, "Repetitive controller for improving grid-connected photovoltaic systems," *IET Power Electron.*, vol. 7, no. 6, pp. 1466–1474, June 2014.

[4] Q. Zhao, Y. Ye, G. Xu, and M. Zhu, "Improved repetitive control scheme for grid-connected inverter with frequency adaptation," *IET Power Electron.*, vol. 9, no. 5, pp. 883–890, April 2016.

[5] Q. Zhao and Y. Ye, "A PIMR-type repetitive control for a grid-tied inverter: Structure, analysis, and design," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2730–2739, March 2018.

[6] Q. Zhao, S. Chen, S. Wen, B. Qu, and Y. Ye, "A frequency adaptive pimr-type repetitive control for a grid-tied inverter," *IEEE Access*, vol. 6, pp. 65 418–65 428, 2018.

[7] B. Han, J. S. Lee, and M. Kim, "Repetitive controller with phase-lead compensation for cuk ccm inverter," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 3, pp. 2356–2367, March 2018.

[8] Z. X. Zou, K. Zhou, Z. Wang, and M. Cheng, "Frequency-adaptive fractional-order repetitive control of shunt active power filters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 3, pp. 1659–1668, March 2015.

[9] Z. Liu, B. Zhang, and K. Zhou, "Universal fractional-order design of linear phase lead compensation multirate repetitive control for pwm inverters," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 9, pp. 7132–7140, Sep. 2017.

[10] B. Zhang, D. Wang, K. Zhou, and Y. Wang, "Linear phase lead compensation repetitive control of a CVCF PWM inverter," *IEEE Trans. Ind. Electron.*, vol. 55, no. 4, pp. 1595–1602, April 2008.

[11] T. I. Laakso, V. Valimaki, M. Karjalainen, and U. K. Laine, "Splitting the unit delay [fir/all pass filters design]," *IEEE Signal Process.*, vol. 13, no. 1, pp. 30–60, Jan 1996.

[12] G. Oetken, "A new approach for the design of digital interpolating filters," *IEEE Trans. Acoustics Speech Signal Proc.*, vol. 27, no. 6, pp. 637–643, Dec 1979.