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A Novel Approach for Three-Phase V/f Induction Motor Drives Employing DC-Link Modulation and AC Chopper

P. N. Tekwani[1],Kinjal Macwan[2] and Patel Vidhi M.[3]
[1,2] Department of Electrical Engineering, Institute of Technology, Nirma University Ahmedabad, India
[3]Silver Oak College of Engineering and Technology, Ahmedabad, India
[1]pn.tekwani@nirmauni.ac.in,[2]14meep16@nirmauni.ac.in,[3]vidhipatel.gn@socet.edu.in

Abstract

This paper proposes a new topology for ac-to-ac power conversion, which is a three-stage conversion. It comprises of a diode rectifier (ac-to-dc), a buck-boost converter (dc-to-dc) and anH-bridge inverter (dc-to-ac) working as an ac chopper. The topology works as V/f drivewherein the frequency is varied by the buck-boost converter and the voltage is varied by the inverter, which is used as a chopper. Thus, it provides variable output voltage and frequency for all three-phases, which can be used for V/f control of induction motor. As compared to the conventional two-stage conversion i.e. ac-dc-ac (ac-to-ac conversion with intermediate stiff dc-link), proposed topology has advantage of improved THD in output voltage, as the input to the inverter is not a stiffed dc but it is a pulsating dc, provided from output of buck-boost converter. Moreover the blocking voltage of each switch of inverter is not constant voltage but varies according to the pulsating input of inverter, thus the stress across switch, as well as machine winding will reduce as compared to two stage conversion system. The proposed scheme offers linear variation of output voltage from zero to rated, avoiding nonlinear overmodulation range used in conventional inverters. The simulation studies are carried out in Matlab/Simulink 2014 and various results are presented.

A. Shukla, J.M. Patel, P.D. Solanki, K.B. Judal, R.K. Shukla, R.A. Thakkar, N.P. Gajjar, N.J. Kothari, S. Saha, S.K. Joshi, S.R. Joshi, P. Darji, S. Dambhare, B.R. Parekh, P.M. George, A.M. Trivedi, T.D. Pawar, M.B. Shah, V.J. Patel, M.S. Holia, R.P. Mehta, J.M. Rathod, B.C. Goradiya and D.K. Patel (eds.), ICRISET2017 (Kalpa Publications in Engineering, vol. 1), pp. 302–315

1 Introduction

A four quadrant dc-to-ac switched mode inverter is analyzed using a buck-boost dc-to-dc converter which intends to be used when ac voltage lower/higher than dc is required, which can be used in UPS design [1]. A dc-to-ac converter topology which is a combination of buck type dc-to-dc converter and a three-phase pulse width modulated(PWM) voltage source inverter(VSI) without use of any passive components in between is created with reduced switching losses which can be used for high frequency applications [2]. AC voltage controllers are widely used for applications such as light dimmers, heat controllers and soft starting in starters, a safe operation is ensured in [3] by using a switching scheme for ac chopper which prevents short circuit. Compared to the dead-time based hard switching, a multiple-step switching technique is used which provides reduced losses [4]. Speed of squirrel cage induction motors can be varied over wide speed range by adjusting its frequency, it finds wide applications in aviation industry [5]. In order to obtain a sinusoidal output voltage even if there are dynamic changes in the input voltage and load current, a topology of ac-ac converter is developed [6]. The conventional ac voltage regulators gave a speed which had lower dynamic response or larger harmonic components, these limitations are overcome by using PWM chopper techniques [7]. There are three operating modes for a buck-boost converter which are - continuous conduction mode, complete and incomplete inductor supply mode, and discontinuous conduction mode, incomplete inductor supply mode [8]. A technique of pulse energy modulation is used for a buck-boost inverter due to which a sinusoidal current is injected into the grid [9]. In order to ensure proper output voltage stability inconditions when the circuit becomes unstable due to variation in resistance of light emitting diode, a closed-loop voltage control system is used [10]. Ripple analysis is carried out for ac choppers in order to design proper input and output LC filter [11]. High voltage spikes due to commutation problems is eliminated by proper switching patterns [12]. The harmonic content in the delivered voltage can be reduced by using particle swarm optimization [13]. The modulation of inverter dc-link is carried out using NXP LPC1768 controller with an aim to obtain a pure sine wave inverter to feed induction motor [14]. A single-phase topology for an ac chopper is simulated and hardware is implemented using dSPACE controller board [15], [16].

The conventional two-stage conversion topology (ac-dc, dc-ac) consist of an intermediate stiff dc-link which provides input to the inverter. Suppose, 415 V of inverter output voltage is needed, then it needs 600V stiff dcvoltage and thus blocking voltage rating of each switch of inverter will be 600V at least, which will increase stress across the switches and lead to high switching losses. In the proposed topology as the dc-link of inverter is modulated so the switches do not require to block a high voltage continuously, but the blocking voltage will vary according to the modulated dc-link. This leads to reduced *dv/dt* stress across switches of inverter and reduces switching losses in return. Moreover, the total harmonic distortion (THD) will be far better than the inverter, which is provided a stiff dc-link voltage at its input.

2 Introduction to proposed topology

The proposed topology consists of an uncontrolled diode rectifier, a buck-boost converter and an inverter connected as shown in fig.-1 [14-15]. Such three units are used to produce a three-phase ac chopper as shown in fig.-2. The input ac voltage is provided to the diode rectifier and the rectified voltage is given as input to the buck-boost converter. Further, the

output of buck-boost is fed to inverter. The buck-boost converter varies the frequency according to the reference frequency provided. The inverter provides voltage control by controlling the duty ratio of gate pulses provided to the switches (working as an ac chopper).

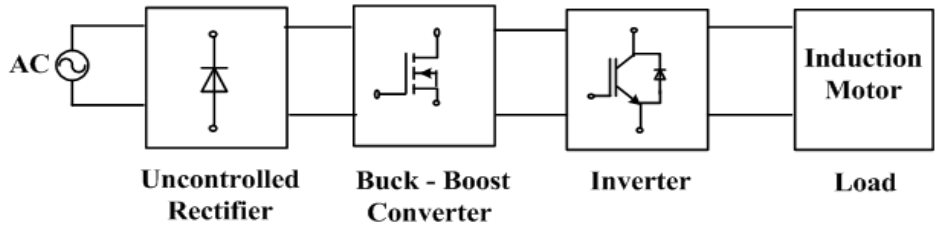


Figure1 Block diagram for single-phase topology

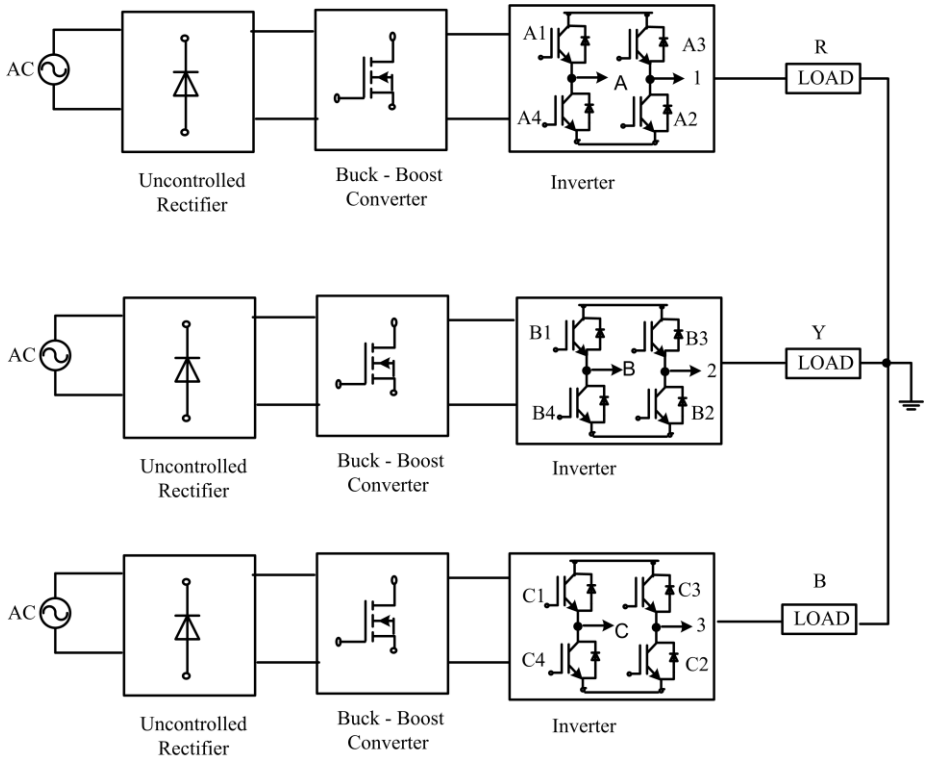


Figure2 Block diagram for three-phase topology

3 Working of Proposed Topology

3.1 Frequency control

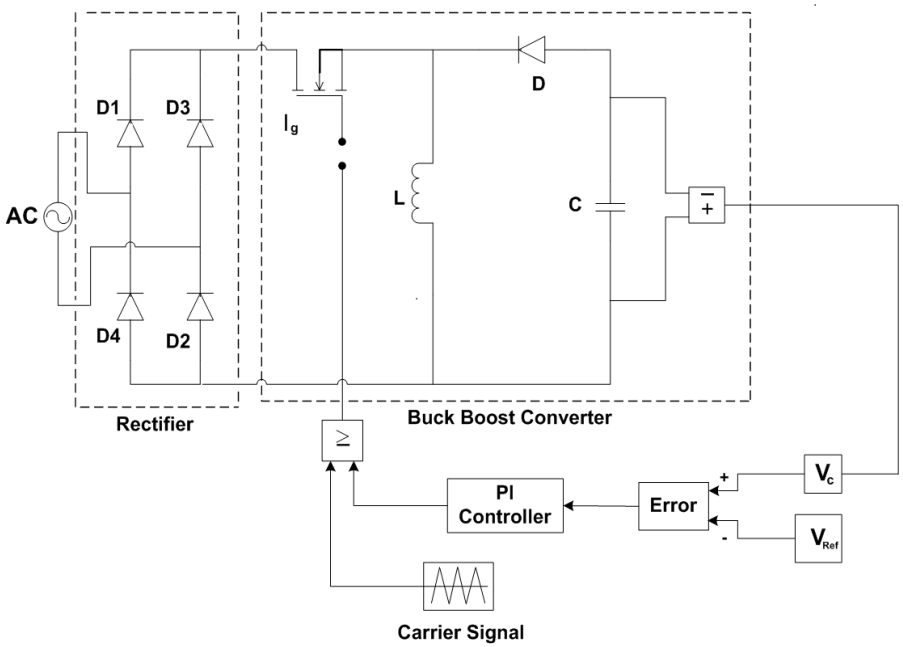


Figure3 Circuit diagram for single-phase topology

As shown in fig.-3 the voltage across the capacitor of buck-boost converter is sensed, and compared with a sine wave of a particular reference frequency, and the error is generated. The error is tuned with the help of a PI controller and compared with a high frequency (10kHz) triangular signal to generate pulses for the switch MOSFET. Refer fig.-4 wherein the input supply voltage (Vinp(A)) is at 800 V, 50 Hz and the reference voltage is at 400 V, 25 Hz. Vc1 (fig.-5) is the actual voltage across the capacitor. The buck mode and boost mode are indicated in fig.-4. Here, as shown in fig.-6 during the buck mode the MOSFET pulses are of very less duty ratio so that the input supply at 800 V will be bucked to 400 V, while during boost mode as shown in fig.-7 the MOSFET is given pulses of high duty ratio so that the voltage will be boosted from (almost) 0 V to 400 V. The closed-loop pulses generated are not of full duty ratio, it is able to boost only up to 200 V from 0 V. Thus the frequency is varied from 0 Hz to 50 Hz with the help of buck-boost converter as explained above.

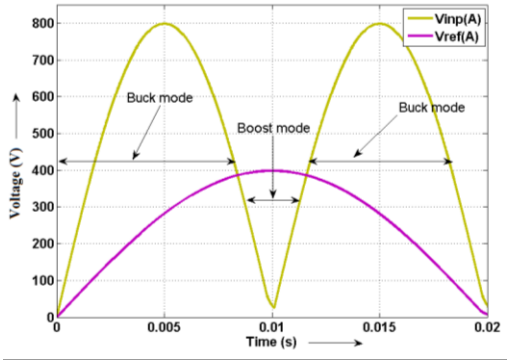


Fig. 4 Energy behavior

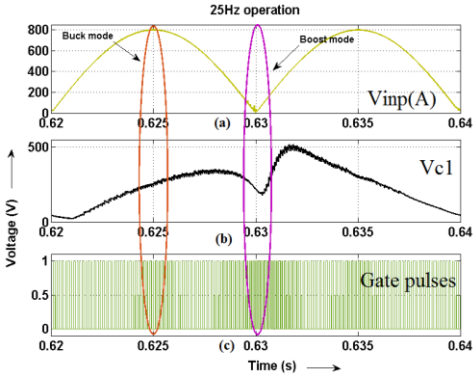


Fig. 5 a)Input rectified supply voltage at 50 Hz (b) Output of buck-boost converter for phase A at 25 Hz (c) gate pulses for MOSFET of buck-boost converter for phase A.

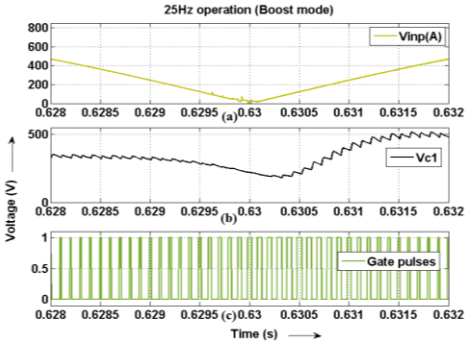


Figure 6 Zoomed view of buck mode from figure-5

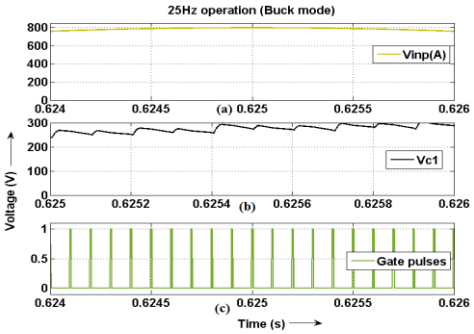


Figure 7 Zoomed view of boost mode from figure-5

3.2 Voltage Control

As the speed ranges from 0 to 1500 rpm, the output rms voltage is varied from 0 V to 230 V (rms) by varying the duty ratio of switches of inverter from 0 to 1 and the fundamental frequency varies from 0 Hz to 50 Hz. Refer fig.-8 for 25 Hz operation which indicates that the V/f ratio ranges linearly with variation in speed i.e. speed ranges from 0 to 750 rpm, frequency from 0 Hz to 25 Hz and duty ratio from 0 to 0.5.Refer fig.-9, where the rms value increases slowly and becomes constant as the speed becomes stable

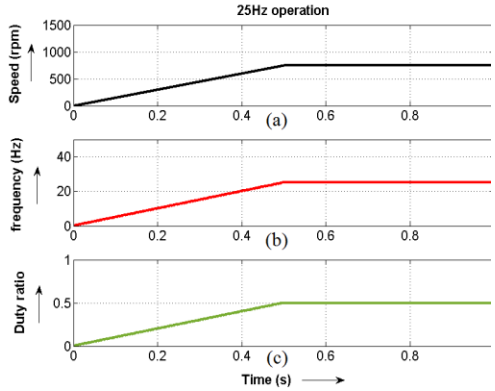


Figure 8 Graph depicting (a) speed (b) frequency and (c) duty ratio variation for 25 Hz operation

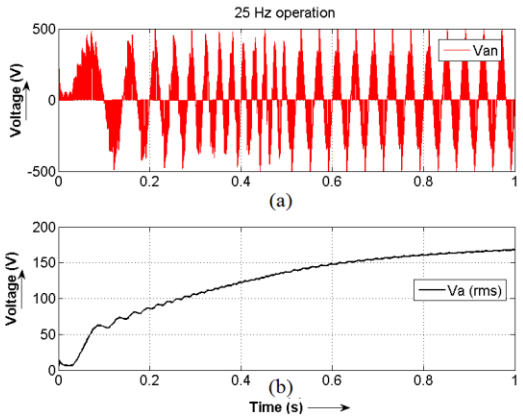


Figure 9 a) Inverter phase to neutral voltage for phase A (b) Inverter output voltage RMS value for phase A

4 Simulation Results

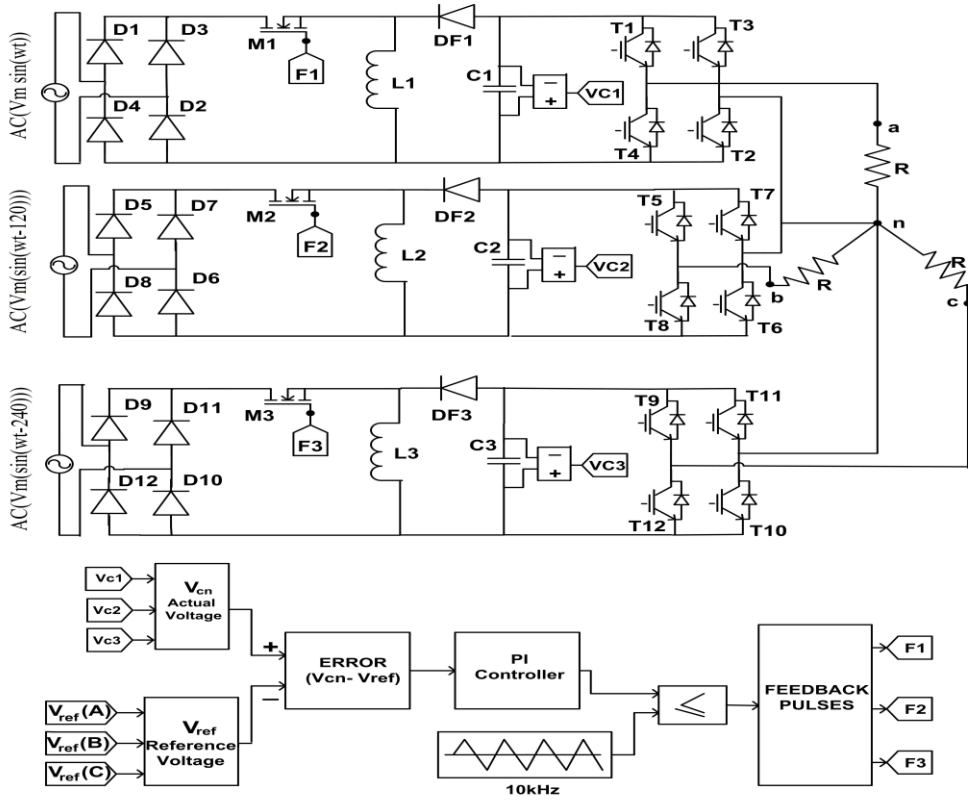


Figure 10 Simulink model for three-phase topology

Table I: Design Specifications

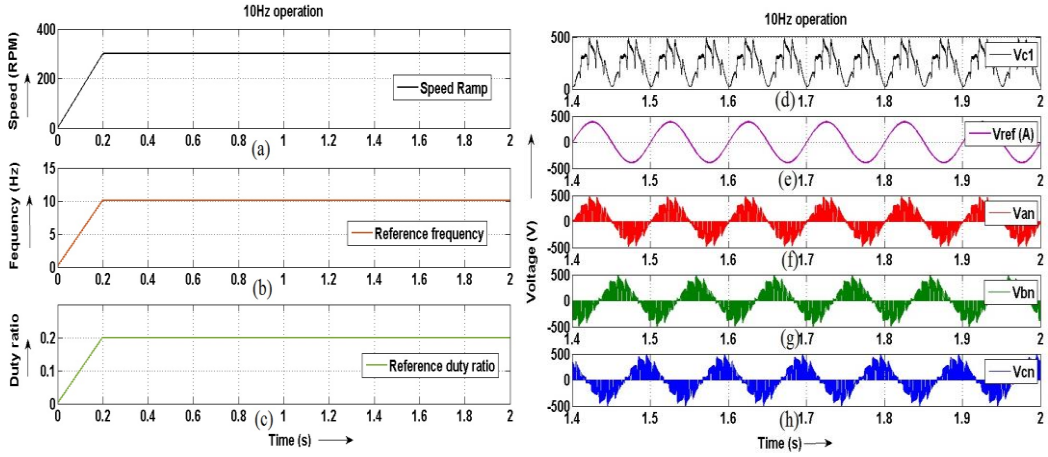
Parameter	Value
Input supply voltage	800 V, 50 Hz
Reference voltage	390 V, 0 to 50 Hz
Carrier wave frequency	10 kHz
Inductance L (L=L1=L2=L3)	0.3 mH
Capacitance C (C=C1=C2=C3)	5 µF

Table II: Acronyms

Acronym	Definition
Vc1	Voltage across capacitor of buck-boost converter
Vref (A)	Reference sine wave voltage signal
Van	Inverter phase to neutral voltage for phase A
Vbn	Inverter phase to neutral voltage for phase B
Vcn	Inverter phase to neutral voltage for phase C
Van(rms)	Rms inverter phase to neutral voltage for phase A
Vinp (A)	Input supply rectified voltage for phase A

Refer fig.-10, which shows the model as created in Matlab/Simulink 2014. The working is same as discussed for the single-phase topology in above section, only the reference and supply voltage sources are phase delayed by 0°,120° and 240° separately. A single closed-loop generates the pulses for all three MOSFETs of the buck-boost converter. Here Vc1, Vc2, and Vc3 are the actual capacitor voltages, V_{ref}(A), V_{ref}(B) and V_{ref}(C) are the three-phase reference voltage and F1, F2, F3 are the MOSFET pulses for each unit. The operation at different reference frequencies are shown in fig. 11 to fig. 13.

4.1 10 Hz Operation



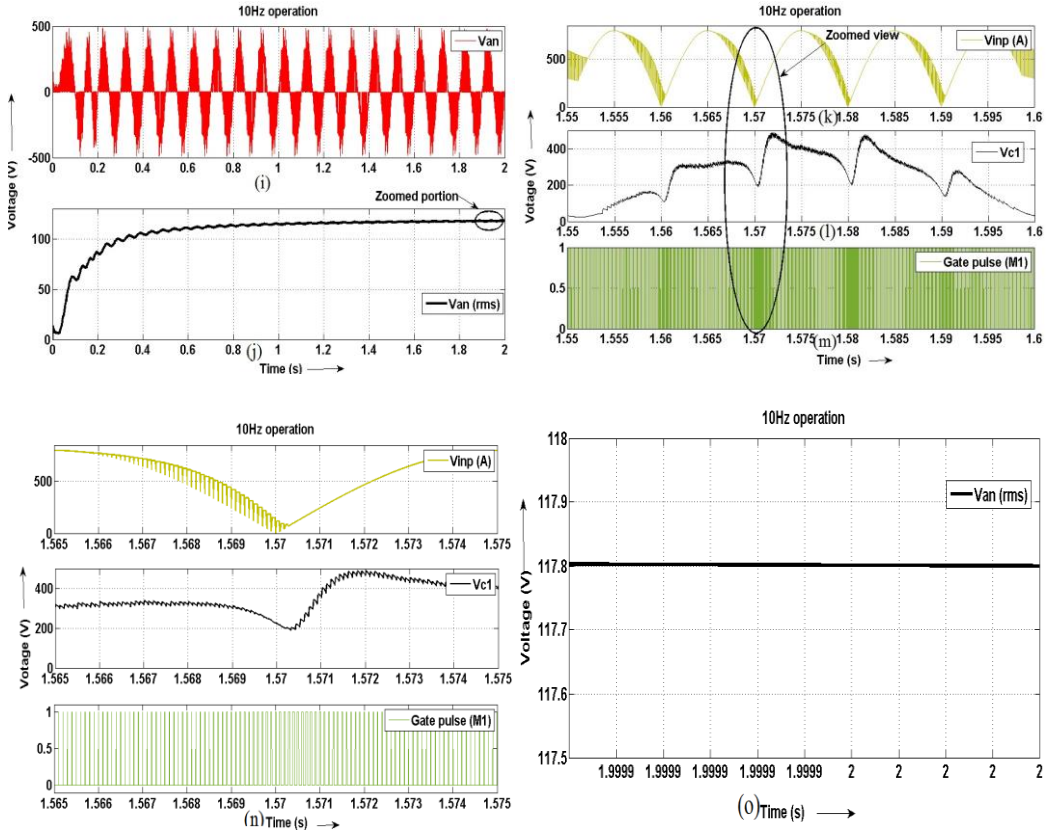


Figure 11: (a) Speed ramp signal (b) Reference frequency (c) reference duty ratio (d) actual capacitor voltage Vc1 for phase A (e) Reference voltage for phase A (f) Inverter output voltage for phase A (g) Inverter output voltage for phase B (h) Inverter output voltage for phase C (i) Inverter output phase to neutral voltage for phase A (j) RMS voltage for phase A (k) Input supply voltage for phase A (l) Actual capacitor voltage (Vc1) for phase A (m) Gate pulse generated through closed loop operation for MOSFET (M1) for phase A(n) zoomed view of fig. 11(k) (o) zoomed view of fig. 11(j)

4.2 20 Hz Operation

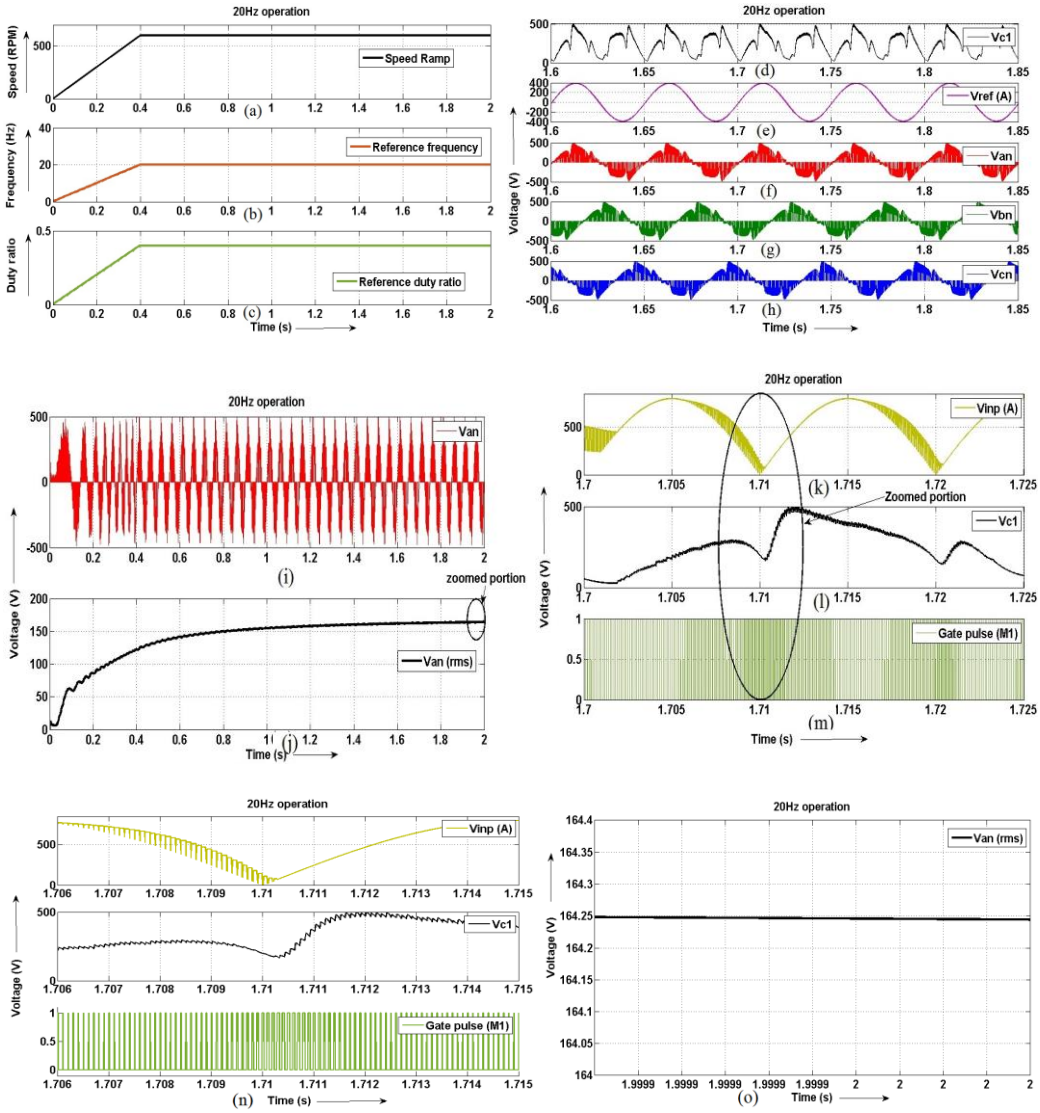


Figure 12: (a) Speed ramp signal (b) Reference frequency (c) reference duty ratio(d) actual capacitor voltage Vc1 for phase A (e) Reference voltage for phase A (f) Inverter output voltage for phase A (g) Inverter output voltage for phase B (h) Inverter output voltage for phase C (i) Inverter output phase to neutral voltage for phase A (j) RMS voltage for phase A (k) Input supply voltage for phase A (l) Actual capacitor voltage (Vc1) for phase A (m) Gate pulse generated through closed loop operation for MOSFET (M1) for phase A (n) zoomed view of figure 12(k) (o) zoomed view of figure 12 (j)

4.3 50 Hz operation

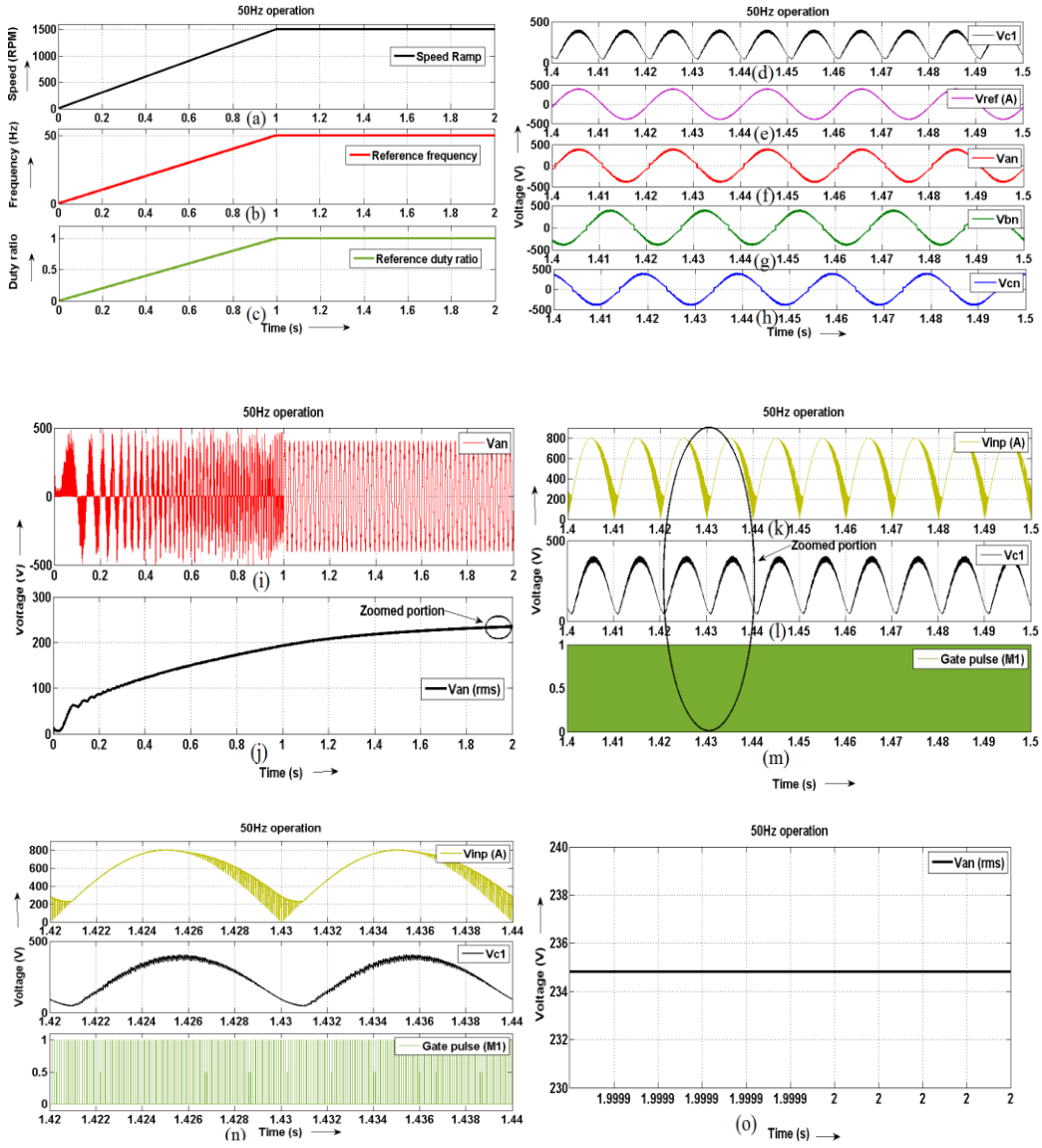


Figure 13 (a) Speed ramp signal (b) Reference frequency (c) reference duty ratio (d) actual capacitor voltage Vc1 for phase A (e) Reference voltage for phase A (f) Inverter output voltage for phase A (g) Inverter output voltage for phase B (h) Inverter output voltage for phase C (i) Inverter output phase to neutral voltage for phase A (j) RMS voltage for phase A (k) Input supply voltage for phase A (l) Actual capacitor voltage (Vc1) for phase A (m) Gate pulse generated through closed loop operation for MOSFET (M1) for phase A (n) zoomed view of figure 13(k) (o) zoomed view of figure 13(j)

5 Explanation for Symmetry Loss in the Output Voltage Waveform of Inverter

When the input supply frequency is at 50Hz and the reference frequency is at 10Hz as shown in Fig. 11, the output voltage of buck-boast converter has symmetry after every 0.05s because the zero crossing of the reference and input supply are coming after every 0.05s, which is shown by bold dots in fig. 14. Such a symmetry in everyhalf cycle will be also obtained when working with reference frequencies of 16.66Hz (fig. 15) and 25Hz (fig. 17),other than 10Hz. When choose reference frequencies are other than these, the waveforms show symmetry, but not in every half cycle. The symmetry is obtained after some half cycles which can be observed by taking reference frequencies at 20Hz, 30Hz, 35Hz, 40Hz, and 45Hz as shown in Fig. 16, 18, 19, 20, and 21 respectively. The bold dots here indicate the zero crossing of input supply signals and reference signals.

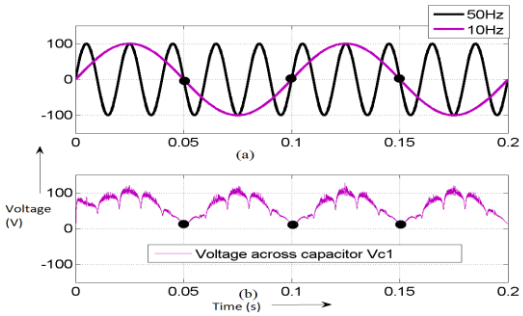


Figure 14 Waveforms explaining symmetry 10Hz

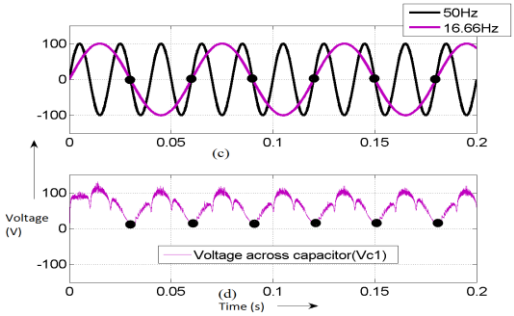


Figure15 Waveforms explaining symmetry at 16.66Hz

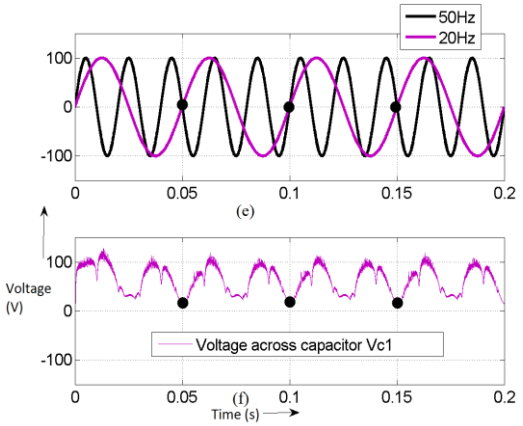


Figure 16 Waveforms explaining symmetry at 20Hz

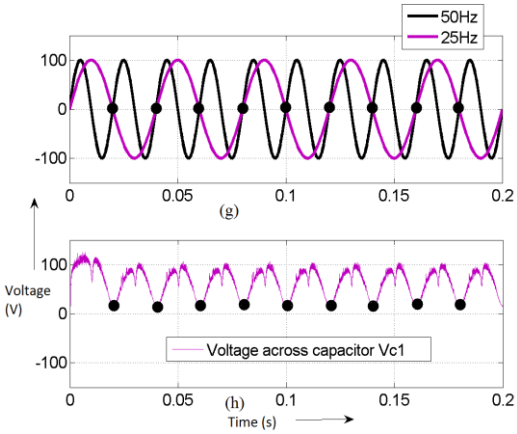


Figure17 Waveforms explaining symmetry at 25Hz

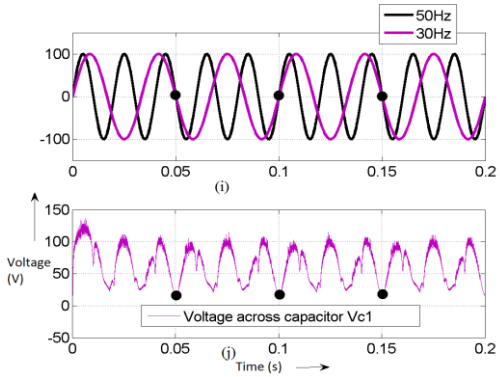


Figure 18 Waveforms explaining symmetry at 30Hz

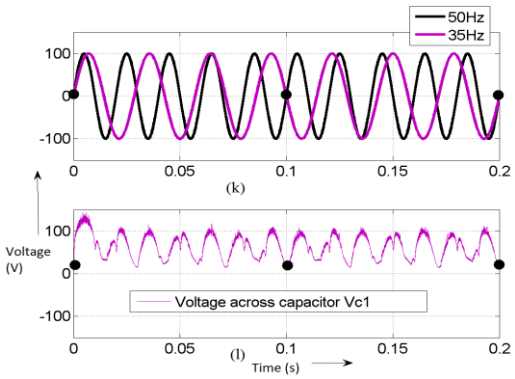


Figure 19 Waveforms explaining symmetry at 35Hz

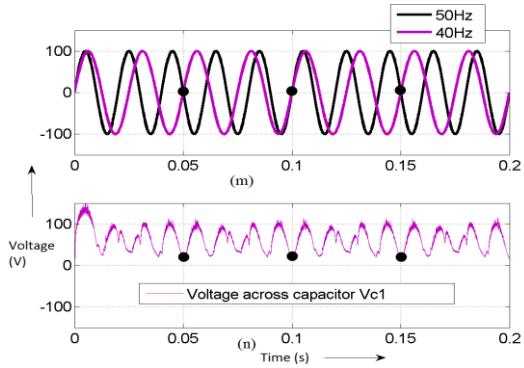


Figure 20 Waveforms explaining symmetry at 40 Hz

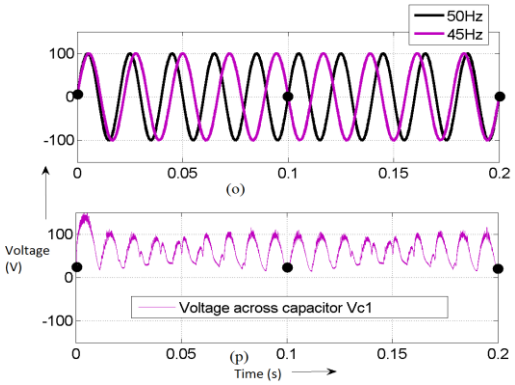


Figure 21 Waveforms explaining symmetry at 45Hz

6 Conclusion

Refer Table III, which concludes for the proposed scheme that as the speed ranges from 0 rpm to 1500 rpm, the frequency and voltage increase linearly keeping V/f constant with the frequency ranging from 0 Hz to 50 Hz and the duty ratio ranging from 0 to 1. As it is evident from Table III, the rms value of inverter output voltage rises, as the duty ratio is increased, and it finally reaches to 235 V rms at 50 Hz as speed becomes stable at 1500 rpm.

Table III: Result Table

Frequency (Hz)	Duty Ratio	Speed (RPM)	RMS voltage (Va rms(V))
10	0.19980	300	117.8
20	0.3996	600	164.25
30	0.5994	900	196.06
40	0.7992	1200	219.5
50	1	1500	235

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